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# CMOS Sensors for Precision Astronomy

James Michael Ivory



A thesis presented for the degree of  
*Doctor of Philosophy*

Centre for Electronic Imaging

School of Physical Sciences

The Open University

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## Abstract

Thanks to rapid development in recent years, CMOS sensors are quickly approaching the performance levels achieved by scientific CCDs. They are now at a point where they are being considered for precision astronomy measurements, such as gravitational microlensing. CMOS sensors offer a number of inherent advantages over CCDs, such as higher frame rate and radiation hardness. In this work, a novel monolithic CMOS sensor capable of full depletion through an applied reverse bias is characterised and tested. Baseline characterisation of basic metrics is undertaken to ensure the device is fully operational. Image lag is measured in the device to determine optimal operating parameters. A novel method for reducing image lag is described and tested, with results indicating a successful reduction. Inter-pixel non-uniformity is investigated to examine the different photo-response from pixel to pixel, as well as intra-pixel non-uniformity to determine the areas of a pixel which are more sensitive to incoming photons than others. The point spread function of the sensor is then tested at multiple reverse biases to ensure that full depletion has been achieved and compared to results taken from a CCD.

## Declaration

I hereby declare that no part of this thesis has been previously submitted to this or any other university as part of any other degree or professional qualification. This thesis has been wholly written by the undersigned, except for colleagues and others acknowledged in the text.

James Ivory

2020

## Dedication

This thesis is dedicated to my family, Kate, and Finn - the best dog in the world.

## Acknowledgments

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## Acronyms and Abbreviations

CCD – Charge Coupled Device

CMOS – Complimentary Metal-Oxide-Semiconductor

MOS – Metal-Oxide-Semiconductor

BSI – Back Side Illumination

WFPC – Wide-Field/Planetary Camera

PPS – Passive Pixel Sensor

IC – Integrated Circuit

QE – Quantum Efficiency

CTE – Charge Transfer Efficiency

PRNU – Pixel-Response Non-Uniformity

NIR – Near Infrared

UV – Ultraviolet

PPD – Pinned Photodiode

STI – Shallow Trench Isolation

FSI – Front Side Illumination

MOSFET – Metal-Oxide-Semiconductor Field-Effect Transistor

SF – Source Follower

ADC – Analogue-to-Digital Converter

FPN – Fixed Pattern Noise

PD – Photodiode

TG – Transfer Gate

FD – Floating Diffusion

SHR – Sample Hold Reset

SHS – Sample Hold Signal

CDS – Correlated Double Sampling

GPU – Graphics Processing Unit

HST – Hubble Space Telescope

UVIS – Ultraviolet-Visible

TDI – Time Delay and Integration

AF – Astrometric Field  
BP – Blue Photometer  
RP – Red Photometer  
LBT – Large Binocular Telescope  
LSST – Large Synoptic Space Telescope  
NTT – New Technology Telescope  
CVF – Charge-to-Voltage Factor  
ADU – Analogue Digital Unit  
FWC – Full Well Capacity  
PTC – Photon Transfer Curve  
DDE – Deep Depletion Extension  
GUI – Graphical User Interface  
ZIF – Zero Insertion Force  
PCB – Printed Circuit Board  
MTF – Modulation Transfer Function  
VKE – Virtual Knife Edge  
PSF – Point Spread Function

# 1 Introduction

## 1.1 Context

Currently, the vast majority of solid-state image sensors used in precision astronomy at ultraviolet, visible and near infrared wavelengths are Charge-Coupled Devices (CCDs). This is due to a number of areas in which they excel, such as good quantum efficiency, near-perfect charge transfer, high sensitivity, and low noise. These are areas in which, traditionally, Complimentary Metal-Oxide-Semiconductor (CMOS) sensors could not compete and so, for over half a century, CCDs have dominated the field.

Recent advancements in CMOS technology have allowed the gap between the two technologies to close significantly. With inherent advantages over their counterpart, CMOS sensors are now beginning to be considered for use in astronomical observations.

Two of the main areas in which CMOS sensors have yet to perform to the levels of CCDs are charge transfer efficiency and lateral charge diffusion. Typical scientific CCDs can achieve transfer efficiencies of over 99.999999%, whereas CMOS sensors can only offer efficiencies (called “image lag”) of < 99%. CCDs are able to be fully depleted, meaning they are able to capture electrons generated throughout their entire depth, even at thicknesses of tens and sometimes hundreds of microns thick. CMOS sensors by design are generally only capable of depleting less than ten microns of silicon, leading to charge being generated in field free regions and spreading from the pixel it was generated in.

This thesis aims to study these two main areas in which CMOS sensors are not currently able to compete with CCDs.

## 1.2 Research Goals

The goal of this thesis is to characterise and investigate a select few metrics of a novel CMOS sensor designed at the Open University. These include:

1. Baseline characterisation of the sensors to ensure full functionality and optimal operating parameters.
2. Measurement of image lag. This includes methods for mitigating image lag.
3. Measurement of the inter- and intra-pixel non-uniformity.
4. Measurement of the point spread function.

### 1.3 Thesis Structure

This thesis is comprised of seven chapters including this one, the introduction.

Chapter 2 provides a brief historical background on the conception and invention of silicon photosensors, both CCD and CMOS. A detailed examination of some of the physics which underpin the operation of the sensors, as well as the semiconductor structures used to create them, is then conducted. The working principles of CMOS pixels are also described.

Chapter 3 consists of a review of current and future observatories, such as the Hubble Space Telescope and the Large Synoptic Space Telescope. This includes both space and ground based telescopes. Advantages of both operating locations are discussed. Background information, science goals and in-depth sensor details are given for each observatory.

Chapter 4 is the first chapter to contain experimental data pertaining to this thesis. It begins with the theory and mathematics of some of the baseline tests used to verify a sensor is working as expected, including gain, linearity, full well capacity and photon transfer curves amongst other metrics.

Descriptions of the sensors used for all data collection in the thesis, as well as the support electronics used for control and data acquisition are provided. This is followed by the characterisation tests used to verify that the sensor is in good working order and its inherent limits.

Chapter 5 describes the measurement of image lag in the devices. Causes of image lag are investigated, as well as some of the current methods used to minimise the effects of image lag.

Details of the experimental procedure used to generate data for image lag are provided. The

influence of the transfer gate, both the voltage applied and the time the voltage is applied for, is investigated, as well as device simulation to probe the location of charge during transfer. A novel method of reducing image lag from charge spillback is presented, as well as results for the new method.

Chapter 6 describes both non-uniformity and point-spread function measurements. Causes of non-uniformity, both between pixels and within individual pixels, are investigated. Causes of lateral charge diffusion, primarily related to absorption and depletion depth are discussed. A description of the optics used, and the mechanical apparatus used for the measurements is provided. Results for inter- and intra-pixel non-uniformity are presented at multiple wavelengths. The point spread function of a CMOS sensor is investigated at multiple wavelengths and compared to a CCD with similar physical attributes.

Chapter 7 is used to summarise the results and findings of the previous chapters. Future work is discussed, including optimisation of the presented work and investigations into unexplained phenomena.

## 1.4 Associated Publications

Stefanov, Konstantin D.; Clarke, Andrew S.; **Ivory, James** and Holland, Andrew D. (2017). Fully Depleted, Monolithic Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias. In: *International Image Sensor Workshop*, May 30-2 Jun 2017, Hiroshima, Japan, pp. 109–112.

Stefanov, Konstantin; Clarke, Andrew; **Ivory, James** and Holland, Andrew (2017). Characterisation of a novel reverse-biased PPD CMOS image sensor. *Journal of Instrumentation*, 12(11), article no. C11009.

Stefanov, Konstantin D.; Clarke, Andrew S.; **Ivory, James** and Holland, Andrew D. (2018). Design and Performance of a Pinned Photodiode CMOS Image Sensor Using Reverse Substrate Bias. *Sensors*, 18(1), article no. 118.

**Ivory, James M.**; Stefanov, Konstantin D.; Turner, Peter and Holland, Andrew D. (2018). PSF and non-uniformity in a monolithic, fully depleted, 4T CMOS image sensor. In: *High Energy, Optical, and Infrared Detectors for Astronomy VIII*, Proceedings, Society of Photo-Optical Instrumentation Engineers, article no. 1070928 (2018).

## 2 Solid State Image Sensors

### 2.1 Introduction

In 1969, there was a strong drive to develop new technologies for digital data storage. A new type of memory was being researched known as bubble memory [1]. This technology was based on storing data in magnetic 'bubbles' on a thin magnetic film, with each bubble representing a bit. At Bell Telephone Laboratories, Willard S. Boyle and George E. Smith were tasked with developing a similar device using semiconductors. They based their ideas on the storage of minority carriers at the silicon-silicon dioxide interface which exists in a Metal-Oxide Semiconductor (MOS) capacitor.

Less than a month later, they had designed and produced a simple version of a modern CCD. The device consisted of nine electrodes, the first of which was used to inject charge and the last to read the charge. The remaining seven electrodes were used to move the charge between these two end electrodes, thus proving the concept of charge transfer[2]. The experiment was a success and formed the foundation for modern solid-state image sensors. For this work, Boyle and Smith were awarded the Nobel Prize in Physics in 2009.

Although this new technology was suitable for image sensing, it was still years away from being viable for scientific purposes. The charge transfer took place at the surface, resulting in poor charge transfer and high noise. It also had a number of deficiencies when compared with competitors at the time, film and imaging tubes, such as low spatial resolution and low sensitivity to UV light. The invention of the buried channel in 1974 at Fairchild Semiconductor helped to remedy the poor charge transfer and reduce the noise associated with surface transfer. At a similar time, RCA developed the idea of Back Side Illumination (BSI) which greatly improved the sensitivity to light, particularly at shorter wavelengths.

By 1974, only five years after their invention, the first commercial CCD became available. By 1977, the first CCD was selected by NASA to be used on a satellite for space imaging. These ended up being

used for the Wide-Field/Planetary Camera (WFPC) on the Hubble Space Telescope. The CCD was chosen for its ability to store charge for a long time, which image tubes could not, for the sensitivity to light, up to 100 times greater than photographic film, and for the very linear response to light.

From this point onwards, CCDs became the detector of choice for scientific imaging, due to their excellent image quality. Further improvements such as the frame transfer CCD have improved image smearing and removed the need for a mechanical shutter. This works by shielding one half of the CCD from photons, called a storage array, and allowing the other, imaging half to collect light. Once the integration period is over, the generated electrons are quickly shifted from the imaging array to the storage array, where they can be read out without any further photogenerated electrons produced. Another technology introduced to the CCD is a gain register added to the readout. This results in the Electron Multiplying CCD, or EMCCD [3]. In this extra register high voltages are applied to certain electrodes to induce avalanche multiplication of the photogenerated electrons, which is very useful in low light applications. This technology allows for noise floors as low as  $0.002\text{ e}^-$  [4].

The invention of Passive Pixel Sensors (PPS) predates the invention of the CCD. In 1967 the first photodetector built using an array of p-n junctions which could each be individually selected and read out was presented [5]. One year later, the source follower was added into the pixel structure, allowing charge-to-voltage conversion in the pixel [6]. The addition of the source follower to the pixel makes them active, giving rise to the Active Pixel Sensor (APS). Due to limitations such as feature size, the complexity of manufacture and high noise, this form of image sensor was largely overlooked. Due to the popularity and relative simplicity of the CCD, it took over two decades for the APS technology to be resurrected and research to begin again in earnest.

As the need for smaller transistors in Integrated Circuits (IC) for computers drove technology sizes smaller, some of the shortcomings of the APS could be overcome. In the early 1990s new sensors were reported, claiming lower power consumption, lower cost and smaller physical size than their CCD counterparts [7]. With the addition of the pinned photodiode [8], the popularity of CMOS

sensors grew exponentially. Due to the low cost, low power consumption and compact size, they soon began being incorporated into consumer products. With the advent of cameras in mobile phones, the market share of CMOS sensors began to overtake that of the CCD. In 2007, the image sensor market share of CMOS image sensors was 54%. By 2012 that had climbed to 74% and by 2017 it had reached 89%, with an estimated 5 billion units produced [9]. With this rapid growth came large investments in CMOS research, both consumer and scientific. CMOS sensors are now at a point where they are being used in space missions [10] due to their inherent radiation hardness.

Despite the rapid growth of CMOS technology there are still a few areas in which it lags behind the CCD. Quantum Efficiency (QE), Charge Transfer Efficiency (CTE), known as image lag in CMOS sensors, and Pixel-Response Non-Uniformity (PRNU) are all areas in which the CCD still has an advantage over the CMOS sensor.

## 2.2 Semiconductor Physics

This section describes some of the basic solid-state structures used to build image sensors and underlying theory thereof.

### 2.2.1 P-N Junction

Although the discovery of the p-n junction occurred earlier, the current-voltage characteristics were largely derived by Shockley in 1949 [11].

A p-n junction is a device with two terminals. They are the building blocks of the vast majority of solid-state electronics, from diodes to transistors and, importantly, image sensors, depending on doping levels, geometry and biasing conditions. The structure of a simple p-n junction is shown in Figure 2-1.



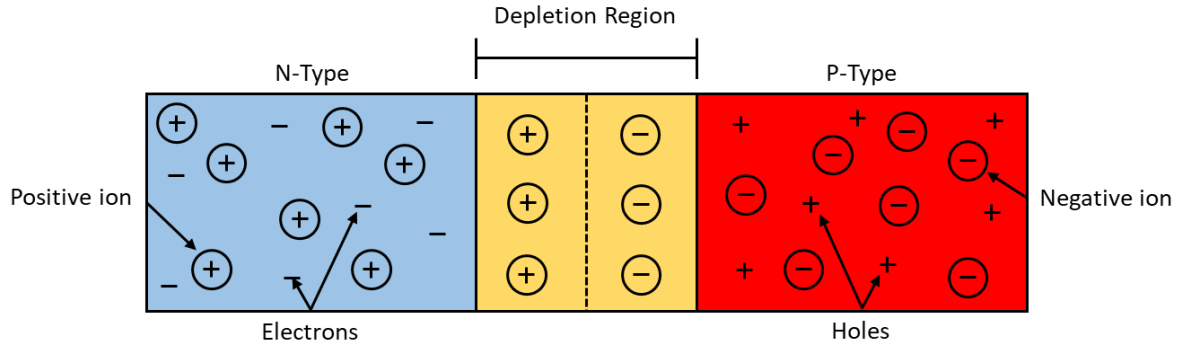


Figure 2-1: P-N junction in equilibrium state with no applied voltages

In its most basic form, a p-n junction is formed with an abrupt junction between a p-type semiconductor and n-type semiconductor. In this thesis we will only consider the case of silicon. N-type silicon is formed by the doping of pure silicon with a donor element, such as phosphorus or another column V element, like arsenic. P-type is made by doping the silicon with acceptor elements, such as Boron or other column III elements. The donor elements get their name from the fact that they contribute mobile electrons to the material. Acceptors contribute mobile holes to the material. These contributions are known as the majority carriers of the material.

When the two types of doped silicon are fabricated on the same wafer such that they are adjacent they form a junction across which majority electrons and holes diffuse. Due to the concentration gradient, electrons will begin to move into the p-type and holes into the n-type sides of the junction. The two charge carriers will recombine, leaving a net charge of zero. With no carriers left, the dopant ions remain in the lattice causing a negative region in the p-type and a positive region in the n-type, the size of which are determined by the concentration of the acceptor ( $N_A$ ) and donor ( $N_D$ ) ions. An electric field is formed which serves to repel the majority carriers from the opposite side of the junction. This is the diffusion potential, or built in potential,  $V_{bi}$ , and its strength is calculated as [12]:

$$V_{bi} = \frac{kT}{q} \ln \left( \frac{N_A N_D}{n_i^2} \right) \quad (2-1)$$

Where  $k$  is the Boltzmann constant,  $T$  is the temperature,  $q$  is the electron charge and  $n_i$  is the intrinsic carrier concentration.

The electric field allow neither holes nor electrons into the region around the junction, known as the depletion region, as it is depleted of all majority carriers. The width of the depletion region,  $W$ , is given as:

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}}{q} \left( \frac{N_A + N_D}{N_A N_D} \right) V_{bi}} \quad (2-2)$$

Where  $\varepsilon_0$  is the permittivity of free space ( $8.85 \times 10^{-12} \text{ Fm}^{-1}$ ) and  $\varepsilon_{si}$  is the relative permittivity of silicon (11.68).

If a positive voltage is applied to the p-type material, and negative to the n-type, the junction is said to be forward biased. In this case, holes and electrons are repelled from the positive and negative voltage sources respectively towards the depletion region. As the voltage is increased, the depletion region will shrink and current can flow due to holes moving one way and electrons moving the other.

Reverse biasing is when the voltages are applied to the opposite ends, i.e. positive to n-type and negative to p-type. In this situation the applied voltage is complimentary to the built-in potential and the electric field is strengthened. Electrons are pulled towards the positive terminal and holes are pulled towards the negative terminal, increasing the width of the depletion region. This increased width of depletion region is very useful for the photodiode in image sensors.

### 2.2.2 Photoelectric Effect

The photoelectric effect is the method by which solid-state image sensors detect light. First described by Einstein in 1905 [13], it describes the emission of free carriers in a material due to the interaction, and energy transfer, with photons. The theory states that a photon with high enough energy will excite an electron enough to free it from its lattice, generating an electron-hole pair. The energy,  $E$ , of a photon is related to its wavelength,  $\lambda$ , as,

$$E = \frac{hc}{\lambda} \quad (2-3)$$

Where  $h$  is Planck's constant and  $c$  is the speed of light.

In silicon the indirect band gap,  $E_g$  is about 1.1 eV. Rearranging Equation (2-3), the minimum wavelength of photon which can be measured in a silicon sensor can be calculated with

$$\lambda_{max} = \frac{hc}{E_g} \quad (2-4)$$

Which gives a value of ~1100nm, beyond which silicon sensors cannot be used for photodetection.

Near InfraRed (NIR), visible and UltraViolet (UV) photons are all below this limit, making silicon sensors suitable for measuring these wavelengths. Below this wavelength, all photons that interact will generate at least one electron-hole pair in silicon. As the energy of the photons increases to values well above  $E_g$ , multiple electrons can be generated from a single photon in silicon. For instance, soft x-rays of energy 5.9keV ( $\lambda = 0.21$  nm) produced by a  $Fe^{55}$  radioactive source will produce 1620 electrons per photon which can be very useful for calibrating devices.

### 2.2.3 Charge Collection Structures

The pinned photodiode (PPD) was the single most important addition to CMOS sensors to bring about its major revival. Originally invented in 1980 and presented in 1982 [14] as a way of decreasing image lag in CCDs, the structure allowed the removal of surface interactions by the generated charge and reduced image lag.

#### 2.2.3.1 MOS Capacitor

The first CCDs were based on surface MOS capacitors. In these structures, a gate electrode is made on p- or n-type silicon, with a layer of silicon dioxide between the two. In the case of p-type substrate, if a positive bias is applied to the gate then the majority carrier holes are all driven away from the silicon-silicon dioxide interface and a depletion region formed. Incoming photons will generate electron-hole pairs and the holes will be swept out of the depletion region. The electron will be drawn into the high potential generated by the depletion region to the surface, where the potential is strongest, shown in Figure 2-2. Any electrons stored here can then be transferred and

measured. As the electrons are stored at the silicon-silicon dioxide interface, they will interact with traps, decreasing the fraction of charge transferred.

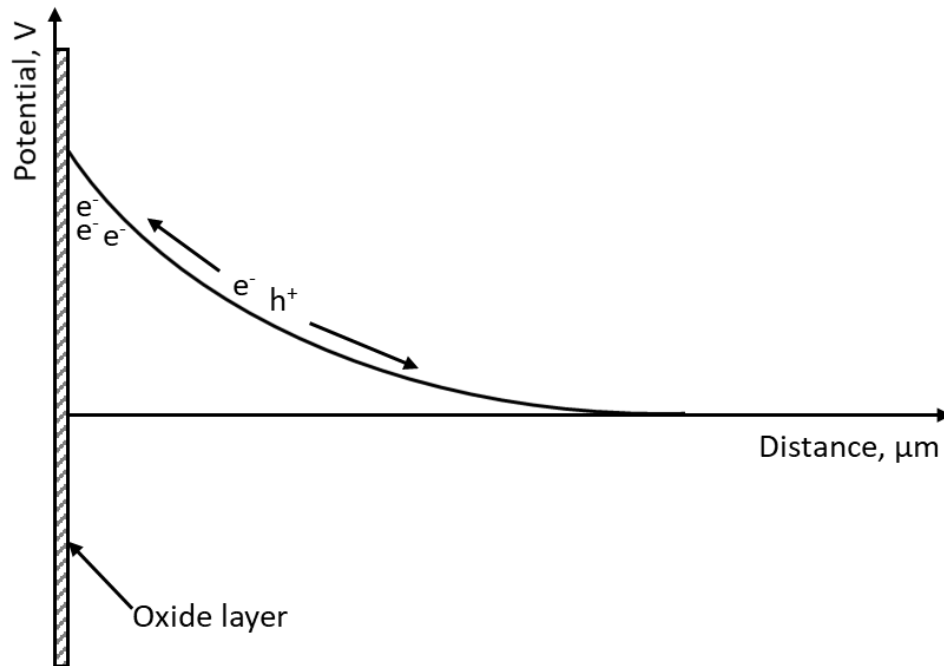


Figure 2-2: Potential diagram of a MOS capacitor under external bias with photogenerated electron-hole pair.

#### 2.2.3.2 Buried Channel

To minimise this effect, the buried channel was invented [6]. The buried channel consists of an extra n-doped layer between the oxide layer and the p-type substrate of a MOS capacitor. In this case, a depletion region is formed intrinsically at the p-n junction with no bias applied to the gate. If there is a voltage difference between the n-region and the gate, with the gate more negative, the electrons will be pushed away from the surface, forming a depletion region as well. When the voltage applied difference is high enough, the surface and p-n junction depletion regions will merge and extend into the p-region, but the maximum potential will be found somewhere in the n-type material, shown in Figure 2-3, because of the uncompensated positive donor atoms. This results in any photogenerated electrons being stored away from the surface, in the buried channel. By applying a larger voltage to the gate, the depletion region can be extended further into the p-type material.

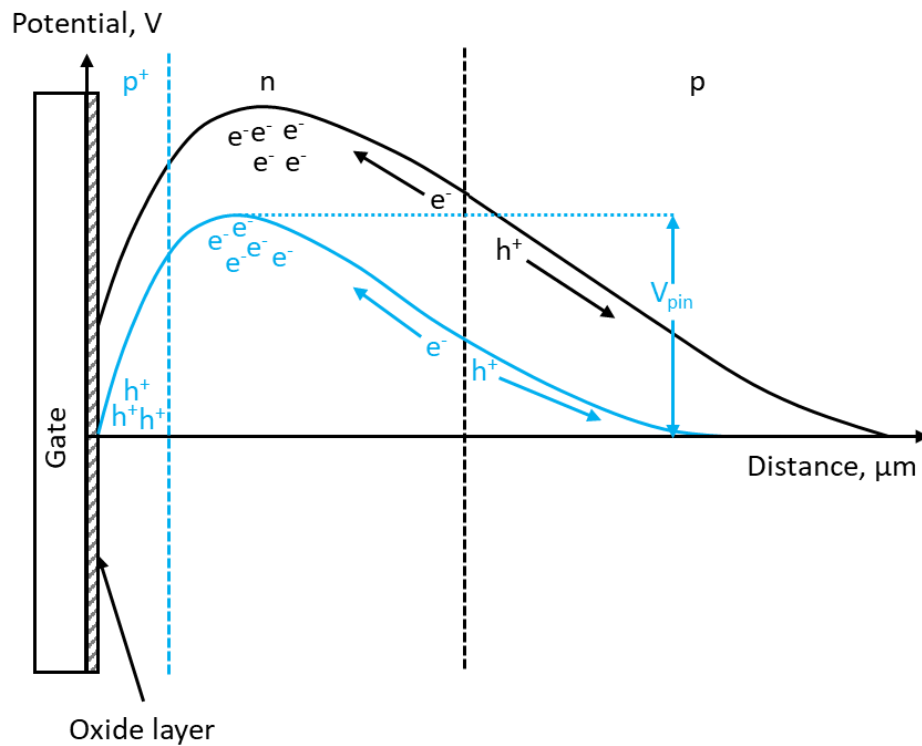


Figure 2-3: Potential diagram of a buried channel photodiode (black) and pinned photodiode (blue), along with the pinning voltage ( $V_{pin}$ ). In both cases it can be seen that the maximum potential is held away from the surface.

### 2.2.3.3 Pinned Photodiode

The pinned photodiode is created by doping the top of the n-type layer with a thin p<sup>+</sup> implant adjacent to the oxide layer. The layout is shown in Figure 2-4. In this, the n-type layer still acts as the collection well for the photogenerated electrons, located between a p<sup>+</sup>- and p-type layer. With current technology, the p<sup>+</sup> layer can be  $\sim 100$  nm thick, the n-type layer 1-2  $\mu\text{m}$  thick and the p-type substrate a few microns thick [15].

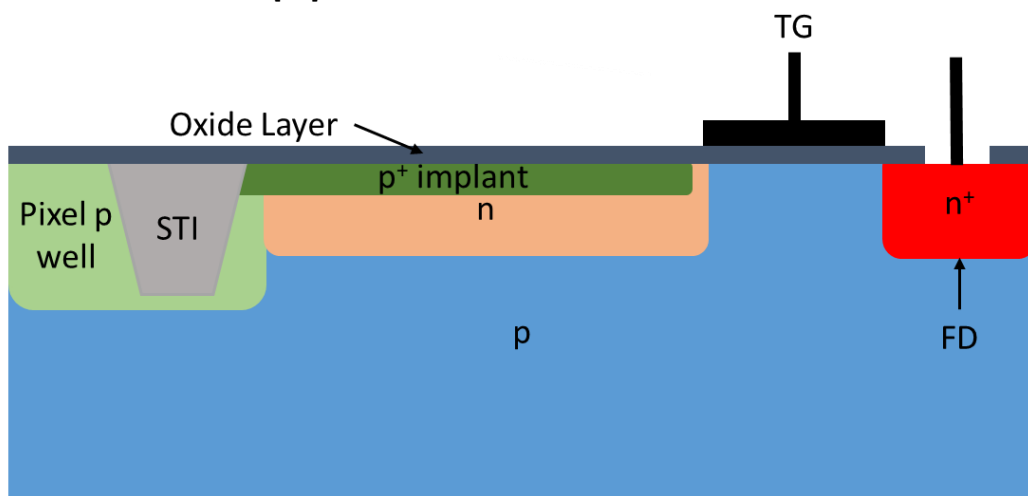


Figure 2-4: Cross section of a pinned photodiode, with the Transfer Gate (TG), Floating Diffusion (FD) and Shallow Trench Isolation (STI) included.

The n-region is intrinsically fully depleted due to the presence of p-n junctions at both the top and the bottom of the layer. This means that no electrode is needed on top of the PPD, so Front Side Illumination (FSI) can be utilised without much attenuation. Careful modifications of the doping profiles of the three layers can be used to extend the depletion region further into the p-type substrate. Generally, increasing the dopant levels also increases the number of charges that can be stored in the PPD. However, doing so increases the pinning voltage, the maximum potential achieved by the PPD when no charge has accumulated. This can reduce the charge transfer efficiency because if the potential is too high, electrons are less likely to be drawn across by the potential of the transfer gate.

Since the collection well is in the n-type material, the electrons are isolated from the silicon surface, eliminating the interaction with surface traps. It is also separated from the shallow trench isolation, another source of surface interaction. The potential in a PPD is similar to that of a buried channel photodiode, except that at the surface the potential is equal to substrate potential. This has the advantage of drawing photogenerated holes to the surface where they can neutralise the surface traps, suppressing dark current. The end result is lower dark signal than in devices which employ a buried channel.

#### 2.2.4 MOSFET

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is the basic building block of most modern electronics. Invented in 1959 by Atalla and Kahng at Bell Laboratories [16], it has since become the most manufactured device in human history, with an estimated  $13 \times 10^{22}$  fabricated by 2018. It can be used for amplifying or switching electronic signals, making them useful for a wide range of applications such as memory, microprocessors and CMOS logic amongst many others. When produced in a CMOS process, both p- and n-channel MOSFETs can be fabricated on the same device.

The structure of an n-channel MOSFET is shown in Figure 2-5. It is created by creating two n-type implants into a p-type substrate, known as the source and the drain. The distance between these two wells is the channel length  $L$ . Each of the two n-regions have a metal ohmic contacts to which voltage may be applied, known as the electrodes. A polysilicon gate electrode is placed above the gap between the two source and drain, separated from the substrate by an insulating oxide layer.

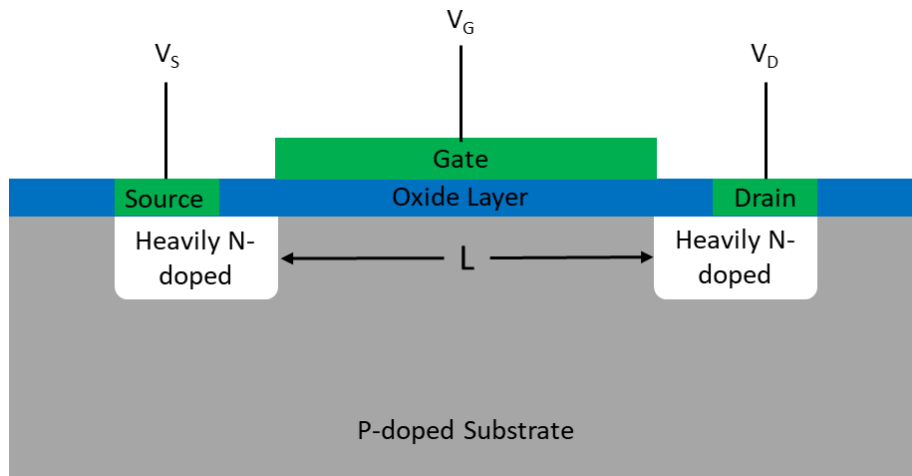


Figure 2-5: Cross section of a MOSFET, with bias voltages illustrated

The source and drain act as two p-n junctions, side by side, with depletion regions forming around them. When no biases are applied, no current flows between the two. If a positive bias difference is created between the gate and source,  $V_{GS}$ , through increasing  $V_G$ , holes are pushed away from the silicon-silicon dioxide interface into the p-material and electrons are drawn to the surface. The mechanism for this is the same as for the MOS capacitor. As the voltage reaches a high enough value, the threshold voltage,  $V_{TH}$ , a surface inversion layer of electrons is formed between the source and drain. As the inversion layer and source and drain have electrons as the majority carrier, a conductive path is formed between the two. The conductance of the layer can be varied by increasing or decreasing the voltage, as long as it remains above  $V_{TH}$ . If a voltage is applied to the drain,  $V_D$ , and the source voltage,  $V_S$ , kept at ground/reference, a current will flow between the two,  $I_{DS}$ . This current can be controlled via  $V_{GS}$ . This is known as enhancement mode operation.

For a sufficiently small drain voltage, the current flow changes linearly with the voltage. The relationship is given as:

$$I_D = \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_{TH}) V_D - \frac{V_D^2}{2} \quad V_D < (V_{GS} - V_{TH}) \quad (2-5)$$

Where  $W$  is the width of the channel,  $\mu_n$  is the carrier mobility and  $C_{ox}$  is the effective gate capacitance ( $\text{Fm}^{-2}$ ).

As the voltage applied to the drain increases, so does the depletion region around the drain. Once the voltage reaches a high enough value,  $V_{Dsat}$ , the depletion region extends under the gate and decreases the channel depth at point Y in Figure 2-6 to zero, known as the 'pinch-off' point.  $V_{Dsat}$  is defined as  $V_{Dsat} = V_G - V_{TH}$ . Once this has occurred, any further increase to  $V_D$  has no effect on the current but will move the point Y closer to the source. This is because beyond  $V_{Dsat}$  the voltage at point Y remains the same and so the number of electrons reaching it will be the same. When electrons reach point Y, they will fall into the drain depletion region, maintaining the current.

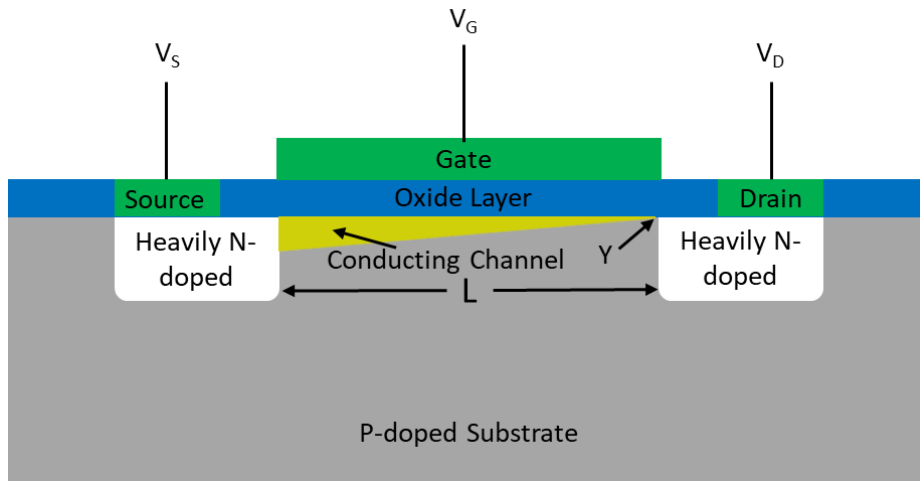


Figure 2-6: Example of pinch-off occurring in a MOSFET when  $V_D > V_{DSAT}$ .

In the saturation regime, only the gate voltage has any major effect on the current flow between the drain and source. The relationship is given by:

$$I_{Dsat} = \frac{mW}{L} \mu_n C_{ox} (V_{GS} - V_{TH})^2 \quad (2-6)$$

Where  $m$  is a function of the doping concentration and can be approximated to  $\frac{1}{2}$  at low doping levels.



If the MOSFET is operated with a gate voltage  $V_{GS} < V_{TH}$ , it is in what is known as the subthreshold mode. In this case, there is no conducting channel formed and no current should flow between the source and drain. A small current can be measured across the transistor due to diffusion of electrons and the magnitude of which is given by:

$$I_D = I_{D0} e^{\frac{V_{GS}-V_{TH}}{kT/q}} \quad (2-7)$$

This mode is how the transistor can be used as a switch – when  $V_{GS} < V_{TH}$ , negligible current flows and the switch is off and when  $V_G > V_{TH}$  and  $V_D < (V_{GS} - V_{TH})$ , current can flow and the switch is on.

MOSFETs, particularly in the saturation mode, are vital to CMOS sensor operations.

## 2.3 CMOS Sensor Design

Using the theory of the basic semiconductor structures from the previous section, this section describes how each is laid out within a CMOS pixel and the roles they fulfil in converting incoming photons to a digital image.

### 2.3.1 Floating Diffusion

The floating diffusion acts as a charge storage area for the electrons after they have been transferred. It is in essence a p-n junction with capacitance  $C_{FD}$ . The capacitance of the floating diffusion is dictated by its physical size and the doping of the p layer.

### 2.3.2 Source Follower

The function of the Source Follower (SF) is to buffer the voltage on the floating diffusion which can be read by an Analogue-to-Digital Converter (ADC).

The source follower is a MOSFET operated in saturation mode. The source of the source follower is connected directly to the drain of another MOSFET, the load transistor, shown in Figure 2-7. This load transistor, acting as a current sink, is also operated in saturation mode and is used to supply a

constant current across both transistors. The current is controlled by the voltage applied to the gate,  $V_{LG}$ , of the load transistor but is kept constant during operation.

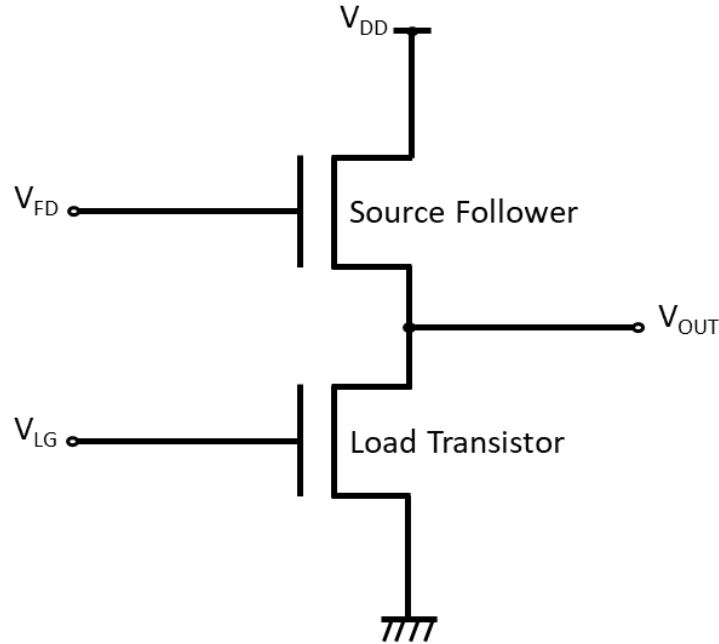


Figure 2-7: Circuit diagram of a CMOS source follower.

If  $V_{LG}$  is kept constant, as well as the voltage applied to the source of the follower,  $V_{DD}$ , any changes to  $V_{FD}$  will induce a change in voltage at its source in order to maintain a constant current. This is because  $V_{GS}$  controls the current in a MOSFET operating at saturation, seen in Equation (2-6). In this case  $V_{GS} = V_{FD} - V_{OUT}$ . Rearranging Equation (2-6) gives the voltage output by the source follower as:

$$V_{OUT} = V_{FD} - V_{TH} - \sqrt{\frac{LI_{Dsat}}{m\mu_n C_{ox} W}} \quad (2-8)$$

It can be seen that the output voltage is linearly related to the voltage applied to its gate. This voltage is supplied by the floating diffusion and is related to the number of electrons stored there by  $V = Q/C$ , where  $Q$  is the charge stored and  $C$  is the total capacitance of the FD.

As there is a source follower in each pixel of a CMOS sensor, any difference in  $V_{TH}$  pixel to pixel will result in slight variations in  $V_{OUT}$  for the same  $V_{FD}$ . These small changes in the threshold voltage

arise from manufacturing inconsistencies in the dopant levels, thicknesses and sizes used. This results in Fixed Pattern Noise (FPN) in images.

### 2.3.3 3T Pixel Architecture

The three transistor CMOS sensor, or 3T, is one of the simplest active pixel CMOS sensor available. It is comprised of a photodiode (PD), a reset transistor, RST, a source follower, SF, a row select transistor, SEL, and a common column bus. The layout is shown in Figure 2-8.

At the start of the integration period, the reset transistor is turned on and the reset voltage  $V_{RS}$  applied to the photodiode, removing any previously generated charge and depleting the junction. The transistor is then turned off and incoming photons generate electrons in the photodiode, reducing the voltage on it. This voltage change is measured by turning on the row select transistor, applying the voltage to the column bus, which in turn is connected to an output for the sensor. This can be converted to a digital signal by an ADC and an image produced. The row select transistor is then turned off and the reset gate pulsed to remove all charge and begin another image cycle.

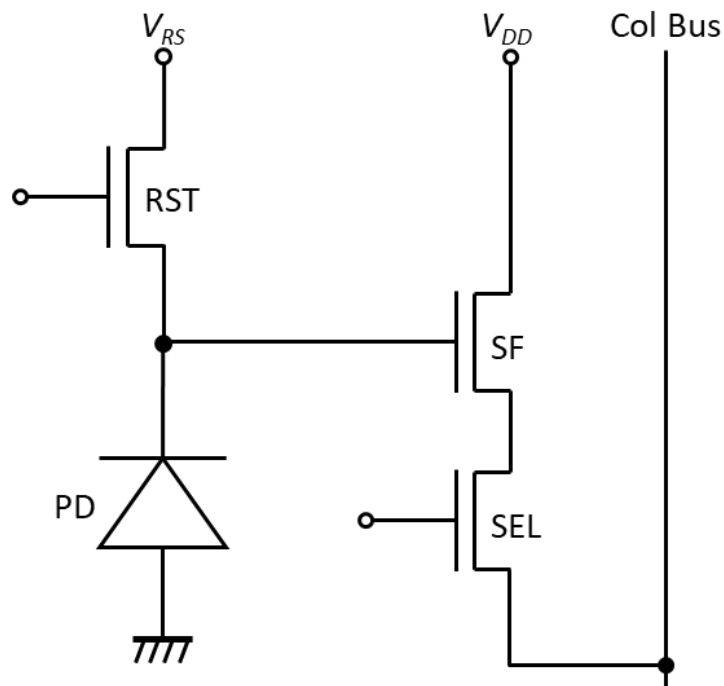


Figure 2-8: Schematic of a 3T CMOS pixel with common column bus included.

The 3T pixel is simple and contains very few elements, making it relatively cheap and easy to reduce pixel size. Few transistors per pixel means a larger photodiode area, increasing the percentage of the pixel sensitive to light, or its fill factor.

3T pixels have a few inherent disadvantages over their more complicated counterparts. These include only being able to operate in rolling shutter mode, which can cause image artefacts from the raster nature of the readout. The output signal always contains the full reset noise, as the photodiode is reset before each imaging cycle. The noise arises from the thermal noise of the channel of the reset transistor and causes the photodiode reset level to differ from the reference voltage. The reset noise  $n_{rms}$ , in  $e_{rms}^-$ , is given by:

$$n_{rms} = \frac{\sqrt{kTC}}{q} \quad (2-9)$$

This cannot be mitigated in a standard 3T CMOS sensor.

#### 2.3.4 4T Pixel Architecture

The four transistor, or 4T, CMOS sensor is the most commonly used architecture for image sensors. It makes use of the pinned photodiode to help reduce dark current and image lag. The extra transistor when compared with the 3T design comes in the form of a transfer gate, shown in Figure 2-10. This allows the readout electronics to be electrically separated from the charge generation area.

### 2.3.4.1 Transfer Gate

The role of the Transfer Gate (TG) is to move the charge generated in the PPD during the integration period to the Floating Diffusion (FD). During charge integration, the transfer gate is biased at zero volts (substrate potential) and it acts as a potential barrier to the electrons, confining them to the PPD. The height of this barrier is equal to the pinning voltage. The barrier height can be further increased by applying a negative voltage to the transfer gate when it is off, increasing the full well capacity of the pixel. During the readout phase, an appropriate voltage is applied to the transfer gate, lowering the potential barrier and drawing the electrons across to the floating diffusion with the generated electric field. Once the transfer period is over, the voltage is returned to zero, creating the potential barrier again for the next integration period. This is shown schematically in Figure 2-9.

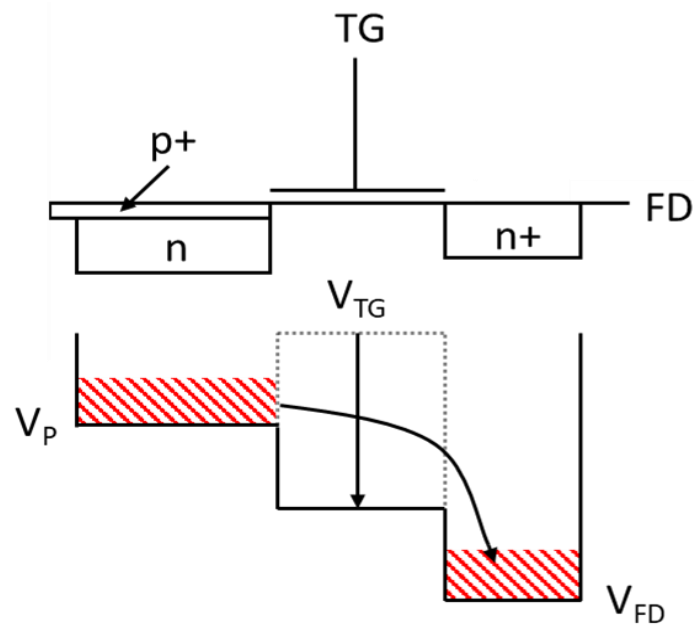


Figure 2-9: Potentials and charge transfer mechanism by the transfer gate.

A more detailed examination of the transfer gate and its effect on charge transfer is provided in Chapter 5.

### 2.3.4.2 Readout

During charge integration, the transfer gate is kept off and charge accumulates in the PPD. Just before the charge is transferred by the transfer gate, the floating diffusion is reset with the reset transistor to the voltage  $V_{RS}$ . The voltage on FD is then measured using the row select transistor and stored on the Sample Hold Reset (SHR) capacitor outside of the pixel. Charge is then transferred, and the voltage measured again. This is stored on the Sample Hold Signal (SHS) capacitor. The difference between these two voltages is the signal from the pixel. Because both signals are stored after the reset pulse has been applied, the reset noise for both will be the same, thus subtracting them removes it. This is known as Correlated Double Sampling (CDS). Although the charge can be transferred in all pixels simultaneously, the 4T pixel still suffers from shutter lag like the 3T pixel due to the raster nature of the rolling shutter readout and reset voltage application.

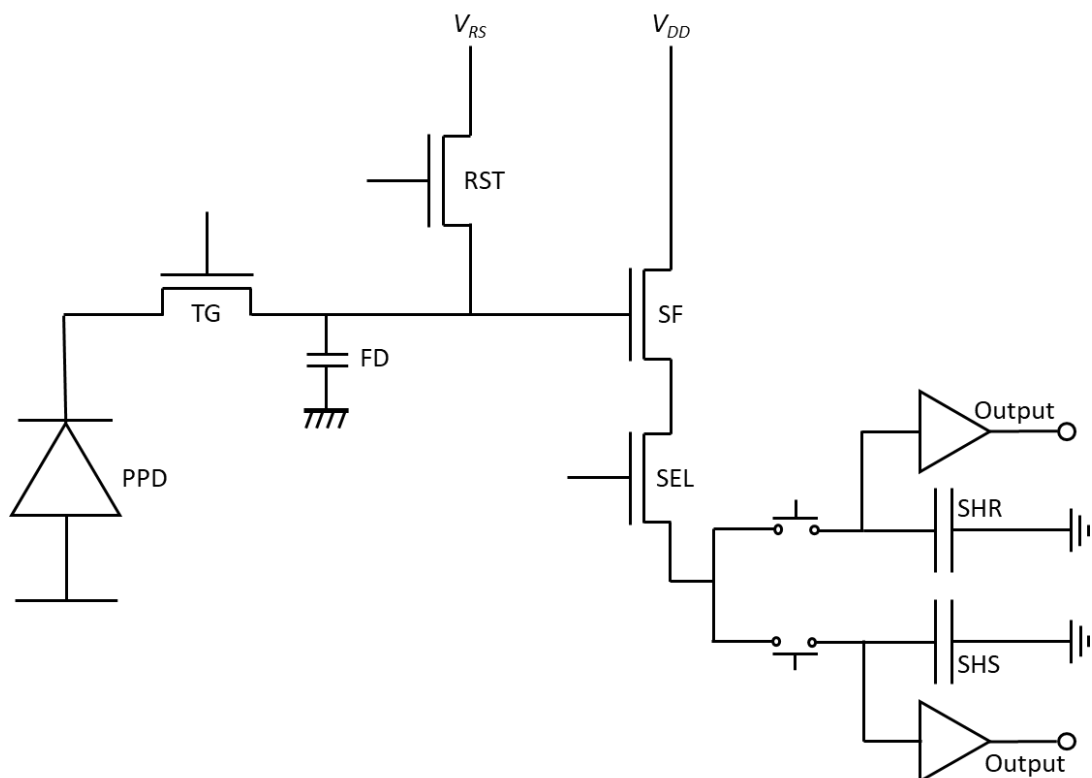


Figure 2-10: Schematic of a 4T pixel, with CDS circuitry included. Note that CDS circuitry is not contained within the pixel itself. Switches used for CDS are electronically controlled.

### 2.3.5 5T Pixel Architecture

The 5T transistor is identical to the 4T, but with an added global reset transistor (GRST) connected directly to the PPD. This allows the PPD to be directly reset at the beginning of the integration period in all pixels at once. This removes any shutter lag found in 3T and 4T pixels as the charge integration and transfer occurs simultaneously for all pixels. This global shutter does however remove the option to perform CDS on the signals from each pixel. This is because when the charge is transferred from all the photodiodes simultaneously the reset level on the floating diffusion is not sampled. CDS can still be enabled on a 5T pixel using global reset, as it is only the global shutter operation which prevents its use.

The 5<sup>th</sup> transistor is shown in Figure 2-11 as GRST.

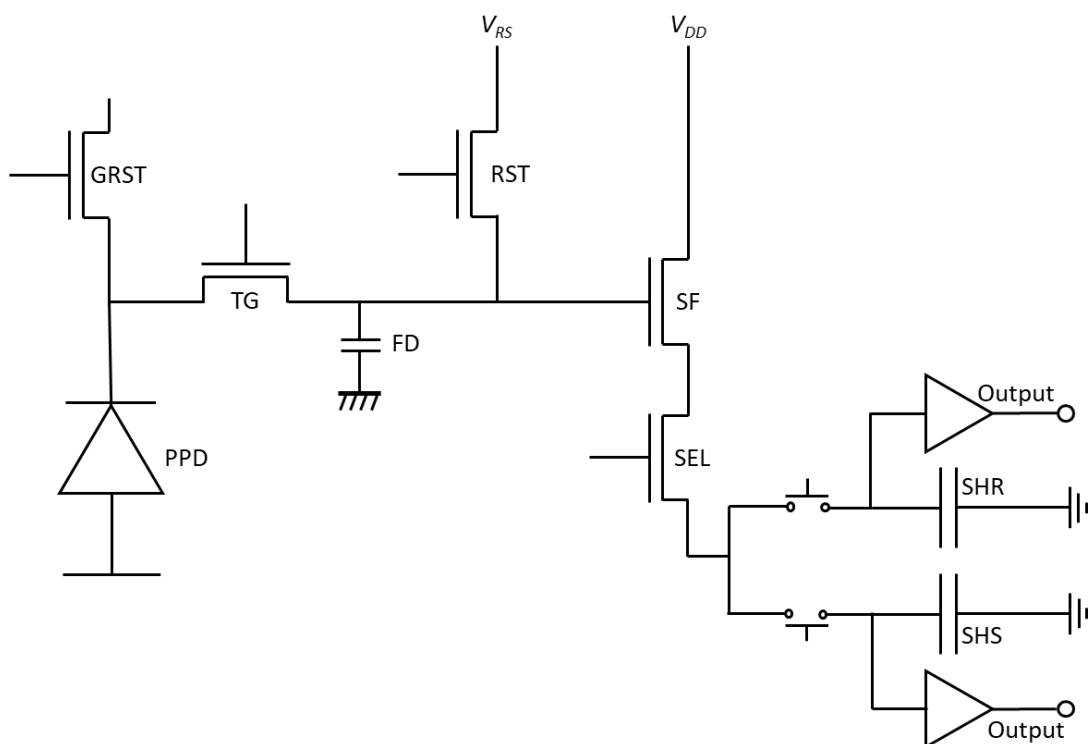


Figure 2-11: Portion of a 5T pixel structure, showing the additional global reset transistor (GRST). The rest of the pixel is identical to the 4T pixel.

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## 3 Solid State Imagers in Astronomy

### 3.1 Introduction

As discussed in the previous chapter, solid state imagers are now the dominant sensors used in both ground and space based astronomical observations. Until recently, CCDs have been the sensor of choice due to their low noise floor [1], higher quantum efficiency [2], more efficient transfer and excellent photo-response uniformity [3]. With recent advancements in CMOS image sensor design and technology, these devices are closing the gap on their counterparts, and there is a growing desire to use the technology in future missions.

This chapter provides an overview of the inherent advantages that CMOS sensors have over CCDs, and provides information on current CCD applications, as well as future CCD and CMOS missions.

### 3.2 Advantages of CMOS sensors

Due to their design and readout mechanisms, CMOS sensors maintain a number of intrinsic advantages when compared with a CCD. Whilst some of these were outweighed in the past by other metrics, recent CMOS sensors can now compete with CCDs and offer uses in areas a CCD would not be practicable.

#### 3.2.1 Radiation Hardness

All space-based telescopes are subject to an amount of harmful radiation [4]. High energy particles in the space environment can cause damage to the lattice structure of the silicon, which manifest as traps for photogenerated charge [5]. These traps will capture an electron from a charge packet, and re-emit them after a certain time, depending on the type of trap [6]. This can result in the captured electron being transferred to a different charge packet, resulting in charge smearing in a CCD. The traps can also increase the dark current of the device.

Due to the way a CCD is read out, a radiation-induced trap can affect an entire column of pixels. If the trap is formed in a pixel near the serial register, the charge cloud in every one of the pixels above

it in the parallel direction will have to pass through this trap. In a large sensor, this could result in thousands of interactions with the trap.

In a CMOS sensor, the charge-to-voltage conversion is handled within the pixel. This means that the charge packet is only ever present in a single pixel. Therefore, any damage will only affect that single charge packet. This is one of the reasons why CMOS sensors are considered radiation 'hard' in comparison with CCDs.

CCDs have a much greater thickness of oxide thickness, ~100 nm, in comparison to those found in CMOS sensors, a few nm. This oxide layer is very susceptible to radiation through ionisation damage. Electron-hole pairs are generated when ionising radiation interacts with the dioxide layer, causing a build-up of charge within. This has the effect of changing the flat-band voltage under the gate electrode. The radiation can also damage the silicon-silicon dioxide interface, removing hydrogen atoms used to passivate the surface, increasing dark current generated by the device. The thin oxide layer of CMOS devices cannot hold enough charge to have a serious impact on the flat-band voltage, but it is still subject to the removal of hydrogen from the interface.

Currently, radiation damage is the largest factor when determining the lifetime of a space mission, so increased radiation hardness can extend the time for which the camera is operational to scientific standards.

### 3.2.2 Power Consumption

In general, a CMOS sensor uses only a fraction of the power when compared with a CCD of a similar sized active area [7]. As well, the necessary support circuits for a CCD consume far more than the internal circuitry of a CMOS sensor. CMOS sensors also run at relatively low voltages (< 5 V) and so all voltages can be supplied from a single source. CCDs require higher voltages for clocking and biasing, often upwards of 30 V. These high voltages necessitate multiple power sources for a single sensor, increasing the volume and mass of the camera system. For space missions, smaller and

lighter components can save weight, and lower power consumption can decrease the need for energy generation and cooling, again saving weight and money.

### 3.2.3 Framerate

Due to the readout method of a CCD, the entire device must be clocked for every image read. This is true even if only a small portion of the pixels are needed for the final image, as the charge in the non-essential pixels will need to be removed. Since each charge transfer takes a finite time to complete, and large devices can require millions of transfers for each image, this results in a low frame rate for CCDs. The transfer times for the unread pixels may be shortened to speed up the process of dumping the unwanted charge, but the pixels of interest must be read out slowly to limit the readout noise from the source follower and other output components. This is because there is only one readout circuit for the whole device, so increasing the readout frequency increases the bandwidth. Johnson-Nyquist noise [8] relates the root mean square voltage  $v_n$  of an electrical circuit to the bandwidth,  $B$ , as follows

$$v_n = \sqrt{4kTRB} \quad (3-1)$$

Where  $R$  is the resistance of the circuit, arising from the resistance from the conducting channel of the MOSFET.

Equation (3-1) indicates that the noise is proportional to the square root of the readout rate, so the rate must be kept low. The readout rate of an entire sensor can be increased with pixel binning with the trade-off of a lower resolution image.

In comparison, CMOS devices containing their own readout circuitry may be selectively read out, with no need to engage the remaining pixels. This gives the advantage of being able to read only a small number of pixels per frame, greatly reducing the readout time. It also reduces the amount of data that each frame contains, which is particularly useful in space-based astronomy when large portions of the image are empty space and the data rate of the downlink to Earth is limited.

The readout of a CMOS sensor is subject to the same Johnson-Nyquist noise as a CCD, but since each pixel has its own readout circuit, the readout can be massively parallelised. An entire row can be read out simultaneously, so can be done slowly whilst still maintaining a high readout rate. With some additional on-chip hardware, CMOS sensors have been shown capable of achieving up to 20 million frames per second for short bursts [9].

EMCCDs can overcome the problem of Johnson-Nyquist noise associated with a greater bandwidth by increasing the signal level to a point where the noise level is negligible in comparison. This facilitates higher framerates at the cost of increased power consumption, as EMCCDs require higher voltages than standard CCDs.

### 3.3 Observation Types

#### 3.3.1 Ground-Based Astronomy

As the name suggests, ground based astronomy is done using telescopes located on the surface of the Earth. There are numerous advantages to ground-based astronomy, but some large disadvantages limit the capabilities of this method.

Firstly, having an observatory on the ground is very cheap in comparison with one in orbit. The cost of launching a rocket with a satellite attached costs upwards of \$50 million as of 2020. This is on top of the cost of the satellite and its components. All of the components must also be certified for use in space, as well as resistant to the vibrations associated with a rocket launch. All of these requirements demand extensive testing which can increase the cost dramatically.

As discussed earlier, any sensor operating in space is subject to large doses of radiation during its lifetime, limiting the operational time of the camera. On the ground, the levels of damaging radiation are practically zero, meaning the technology is the only limiting factor on the lifetime of the observations. It also reduces the need for characterisation of the sensors under high doses of

radiation, lowering the cost and time of the design and test phases. With less radiation damage, the images produced also will need fewer corrections to produce the final image.

With the telescopes accessible at all times, maintenance is an easier task in comparison with space-based telescopes. Any faults can be remedied almost instantly and with only the cost of the components needed. For orbiting satellites, repair missions incur great costs due to rocket launches and can take months to prepare and carry out [10], with the added risk of the loss of human life.

Larger diameter mirrors can be used on the ground than in space due to laxer weight restrictions and the lack of damaging vibrations. Larger mirrors can capture more light than smaller ones, decreasing the integration time of images and increasing the number of images captured over a specific timeframe. Larger optics can also produce better magnification results.

All equipment used in the observatories can be connected directly to the grid power of the local area. This includes the sensors, telescope movement apparatus, control electronics and data storage and processing computers. This allows for far more powerful components to be used without fear of running out of power. It also allows for much larger volumes of data to be obtained as there is a physical connection between the camera and processing computers, permitting a much higher data rate than space-based communications. Full, uncompressed images can be stored or even analysed in real time. GravityCam for example has a predicted data output of ~400 TB per night when operational [11], compared with the Hubble Space Telescope generating 80 GB of data a month. One solution for this large amount of data is to perform analysis on it in real time with multiple Graphics Processing Units (GPUs), something which could not be done in orbit.

Despite all of these advantages, ground based observatories lack in the most critical of metrics – the images they produce. Any astronomy image taken from an Earth based system measures light after it has passed through more than 100 kilometres of air in the atmosphere. The density of the air varies with altitude, and the different densities have slightly different refractive indexes, bending the light as it travels, known as atmospheric aberration. This can produce smeared images of point

sources, changing the measured size and shape of the object and reducing the angular resolution of the system [12]. The effect of this smearing can be minimised through software, with the application of lucky imaging [13], or hardware, with adaptive optics [14].

Imaging from the ground is also only possible at night. This limits the number of hours in which observations can be made. It is also only possible if the sky is clear, as any cloud cover will block light from the objects which are being studied, further reducing the observation window. The effects of these natural phenomena cannot be reduced in any way. Light pollution from nearby towns and cities can also increase the background signal, essentially adding another noise source. Both atmospheric aberrations and light pollution problems can be minimised by building the observatory in a remote location at high altitude, reducing the seen thickness of the atmosphere and reducing the sources of external light.

### 3.3.2 Space-Based Astronomy

For precision astronomy, space-based imaging systems offer the best, most reliable option. Even after considering all of the extra costs and trade-offs which must be made in comparison with ground-based telescopes, they still offer the greatest value for money.

As the observations are made from outside of the atmosphere, they are unaffected by both cloud cover and atmospheric aberrations. They are also pointed away from the Earth and Sun, so are not affected by light pollution or the day/night cycle. With these limitations removed, it is possible to image continuously which facilitates the imaging of very distant or dim objects with integration times of many hours.

The Earth's atmosphere is very absorbent to high energy photons, as well as infrared, making observations of them impossible at ground level. Space-based telescopes can image these wavelengths before they interact with the atmosphere. Current missions include infrared, x-ray, ultraviolet and gamma ray imaging.

The majority of the observatories in space currently are in Low Earth orbit (< 2000 km) with some orbiting at a greater distance. Future missions are tending towards Halo orbits, or orbits around the Lagrange point  $L_2$ , where the Earth and Sun are always aligned with respect to the satellite. These make shielding from solar wind easier as one side of the satellite is always facing the sun and the sensor can be mounted on the opposite side. It also allows for passive cooling of the sensor down to 50 K.

### 3.4 Current Astronomy Missions

#### 3.4.1 Hubble Space Telescope

Although not the first space telescope [15], the Hubble Space Telescope (HST) is by far the most famous and successful. Plans for a large space telescope begun in earnest at NASA in 1968, with a speculated launch in 1979. Due to funding delays and construction setbacks, the eventual launch date was pushed back over time to 1990. It was launched into Low Earth orbit on April 24<sup>th</sup> with an estimated total cost of \$4.7 billion. The running and servicing costs since launch to 2010 have brought up the total cost to around \$10 billion.

The science goals of the mission were very broad, ranging from observations of Mars to detecting the furthest objects in the observable universe. The main precision astronomy goals for the HST are as follows:

- Stellar Archaeology – studying the earliest stars in the universe. Examining the atomic abundances in these stars can give an insight into how the stars were formed, supernovae and nucleosynthesis. Observations of this type are made in the visible and ultraviolet wavelengths.
- Distance of galaxies with high red shift – These measurements are done either through parallax or brightness comparisons. Observations are made at visible and ultraviolet wavelengths.

- The highest redshift galaxies – The study focusses on galaxies which are moving away from Earth at the highest velocity. Observations are made with an infrared sensor as the wavelength has been redshifted.
- Galactic Evolution – studying how galaxies form and shape. Studying galaxies at different distances from Earth can give insight into different stages of their development. Observations are conducted across all wavelengths.
- Stellar birth, death and the interstellar medium – Observing proto-stars and supernovae, as well as the gasses found in space between stars.

Along with these, the HST has given a more accurate value for the Hubble constant, and thus the age of the universe, the accelerating expansion of the universe, the mass of the Milky Way and much more. Over 15,000 papers have been published in peer reviewed journals using data from the HST. The mission is expected to continue producing valuable scientific data until 2030-2040.

To make these observations there are a suite of sensors in the focal array. The main astronomy sensors are the Ultraviolet-Visible (UVIS) camera and the Near Infrared (NIR) camera. The NIR camera is fabricated on HgCdTe, so will not be discussed further. The specifications for the UVIS camera are given in Table 3-1 [16]. The sensors were manufactured by e2v Ltd and are back-illuminated and back-thinned to increase the UV quantum efficiency. The serial register is located on the long side of the sensor to minimise the number of parallel transfers needed, decreasing the impact of the charge transfer inefficiency, shown in Figure 3-1. The low readout noise and high full well capacity contribute greatly to the mission's success. The quantum efficiency values, while low, do not have a great impact on the image quality as space telescopes can account for this with longer integration times.



Characteristic	Value
Type	CCD43
Format	2 arrays of $2051 \times 4096$ pixels
Pixel Pitch	$15 \mu\text{m} \times 15 \mu\text{m}$
Spectral Range	200 to 1000 nm
Noise	$3.1 - 3.2 \text{ e}^-$
Dark Signal	$9 \text{ e}^-/\text{hour}/\text{pixel}$ at 190 K
Quantum Efficiency	50–59% @ 250 nm 68–69% @ 600 nm 47–52% @ 800 nm
Gain	$1.55 \text{ e}^-/\text{DN}$
Full Well Capacity	$63,000 - 72,000 \text{ e}^-$

Table 3-1: Sensor metrics for the UVIS onboard the HST.

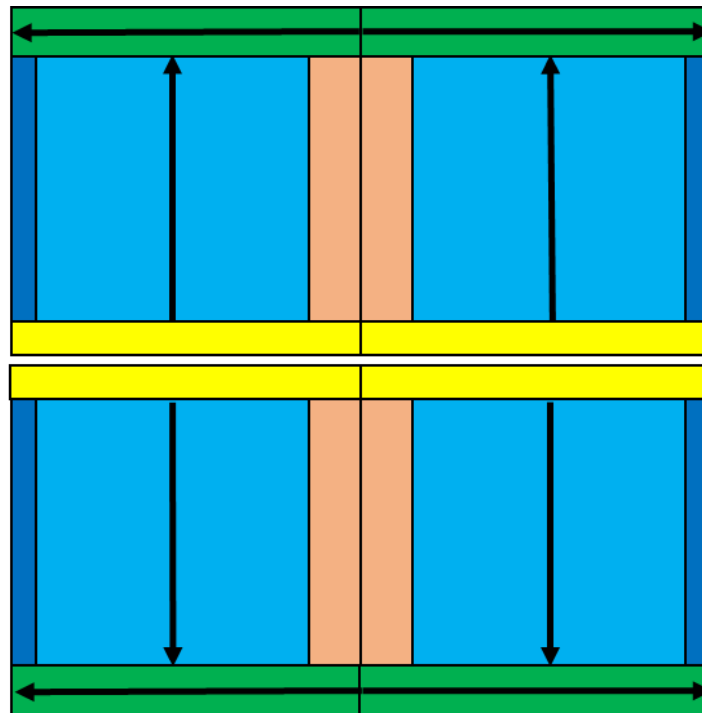


Figure 3-1: Focal plane array of the UVIS camera on the HST. Light blue sections are the imaging area, green is the serial register, dark blue is physical serial overscan, yellow is parallel virtual overscan and orange is virtual serial overscan. Physical overscan is comprised of pixels not exposed to light. Arrows indicate direction of charge movement during readout.

### 3.4.2 Gaia

The Gaia space telescope was proposed by ESA in 1993 as a successor to its earlier Hipparcos mission. Adopted in 2000, it was launched in 2013 with an estimated cost of \$1 billion.

The main science goals for the mission are:

- Measure the position of one billion stars, the accuracy of which is based on the brightness of the star
- Measure the distance to 20 million stars with an accuracy of 1%, and 200 million more with an accuracy of 10%
- Measure the speed of 40 million stars to within 0.5 km/s
- Derive atmospheric parameters and atomic abundances in stars
- Detect up to half a million quasars

All of the sensors used in the Gaia focal plane are custom designed and manufactured by e2v Technologies. They are CCD91-72, which are back-illuminated and back-thinned full-frame CCDs, run in Time Delay and Integration (TDI) mode. There is a total of 106 of the sensors organised as shown in Figure 3-2 [17].

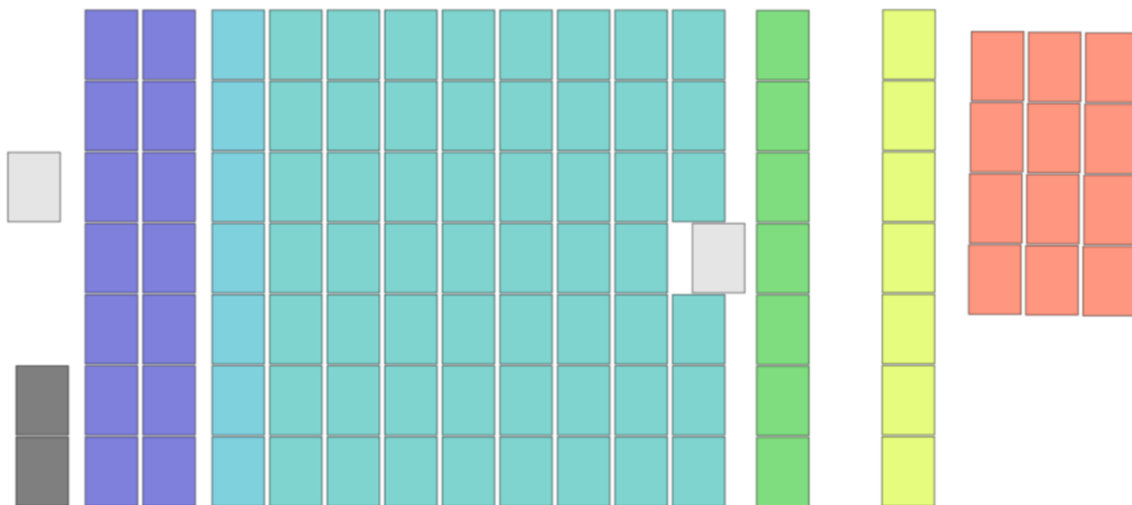


Figure 3-2: Focal plane arrangement in the Gaia space telescope. Light grey represents the two wave front sensors, dark grey the basic angle monitor, purple for onboard detection, light blue for astrometric field, green for blue photometer, yellow for red photometer and red for radial velocity spectrometer.

The entire focal plane has a combined surface area of  $0.5 \text{ m}^2$  ( $1 \text{ m} \times 0.5 \text{ m}$ ). The main astronomy sensors are the Astrometric Field (AF), Blue Photometer (BP) and Red Photometer (RP). These all vary slightly in design to match the needs for the wavelength they are measuring. Both AF and BP devices are back-thinned to  $16 \text{ }\mu\text{m}$  to increase quantum efficiency at shorter wavelengths. They also

have anti-reflective coatings centred at the wavelengths they will be measuring (650 nm for AF, 360 nm for BP). The RP sensor is fabricated on high-resistivity, deep-depleted silicon, thinned to 40  $\mu\text{m}$  to increase the red response and has an anti-reflective coating centred at 750 nm. Specifications for the sensors combined are given in Table 3-2.

Characteristic	Value
Type	CCD91-72
Format	106 arrays of $4500 \times 1966$ pixels
Pixel Pitch	$10 \mu\text{m} \times 30 \mu\text{m}$ rectangular
Spectral Range	330 to 1050 nm over all sensor variants
Noise	6.6 $e^-$ for AF 7.3 $e^-$ for BP and RP
Full Well Capacity	190,000 $e^-$

*Table 3-2: Metrics for the main astronomy sensors onboard Gaia.*

For this mission, the high full well capacity and low noise values are essential for making accurate brightness measurements as both bright and dim stars will be present in the images and so a wide dynamic range and high signal to noise ratio are essential.

### 3.4.3 Large Binocular Telescope

The Large Binocular Telescope (LBT) [18] is a ground-based observatory located on Mount Graham, Arizona in the United States, situated 3,300 m above sea level. It is a combined effort with contributions from Italy, Germany and the United States and was completed in 2004. The total cost of production was around €100 million.

It is unusual in that it employs two separate telescopes, on a common mount in tandem to observe an object at different wavelengths simultaneously. The light collected by the separate mirrors can be used individually or combined to create one high-resolution image. The two mirrors used to focus light combined make it one of the largest telescopes in the world. The combination of the mirrors

also allows detail in the measurements than would be possible from a single mirror of larger proportions.

The telescope utilizes adaptive optics to counteract the effects of atmospheric aberration, increasing the sharpness of the images, with measured sharpness surpassing that of the HST at certain wavelengths.

The main science goals of the telescope are to compliment data from other surveys done on smaller telescopes. The main imaging areas are:

- Wide field surveys in which near-ultraviolet and near-infrared can be run in parallel using the two mirrors.
- Deep photometry of stars found in dwarf galaxies orbiting the Milky Way. The large aperture of the telescope allows for imaging of faint objects.
- Observing variable or transient objects. The high sensitivity of the telescope and sensors combined allows for shorter exposures, increasing the temporal resolution. An example is the short optical afterglow following gamma ray bursts [19].

To measure at two wavelengths simultaneously, two separate sensor arrays are required. One array is optimised for shorter wavelengths whilst the other is optimised for longer wavelengths. Each array consists of 4 CCD42-90s, butted together which cover 75% of the field area, shown in Figure 3-3. The focal plane array also contains two smaller CCD42-10 sensors for tracking and wave front analysis. For the measurements being conducted by this telescope, high quantum efficiency, full well capacity and low noise are crucial for accurate results. Characteristics of the devices are shown in Table 3-3.

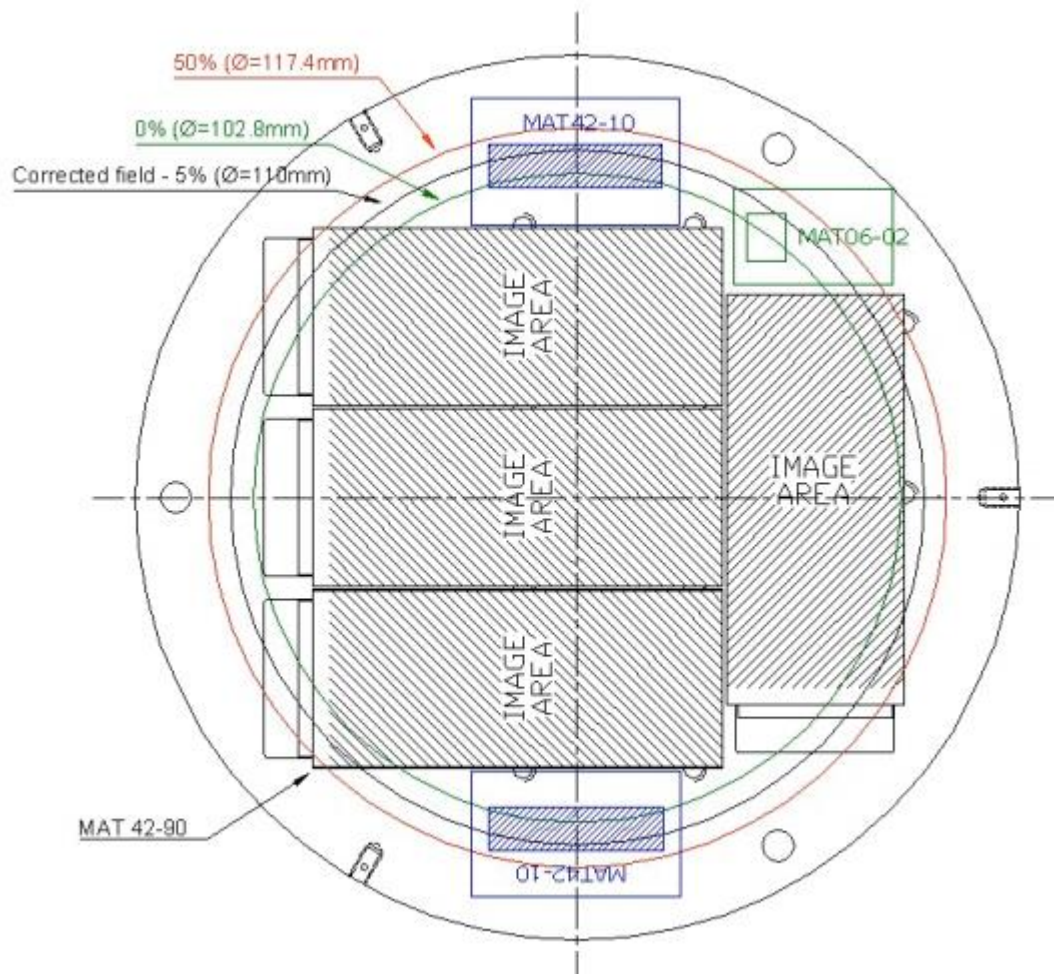


Figure 3-3: Focal plane array arrangement of one side of the LBT. Both sides are identical.

Characteristic	Value
Type	CCD42-90
Format	4 arrays of 2048 × 4608 pixels
Pixel Pitch	13.5 $\mu\text{m}$ × 13.5 $\mu\text{m}$
Spectral Range	350 to 1000 nm
Noise	< 5 $e^-$
Dark Signal	< 1.5 $e^-$ /minute at 170 K
Quantum Efficiency	78–84% @ 400 nm 90–96% @ 600 nm 51–57% @ 900 nm
Gain	4.5 $\mu\text{V}$ / $e^-$
Full Well Capacity	150,000 $e^-$

Table 3-3: Metrics for the two sensors in the Large Binocular Telescope.

### 3.5 Future Astronomy Missions

This section outlines some of the astronomical observatories which are either in the design phase or due to be launched/commissioned in the future. A brief outline of their science goals and sensor information is given.

#### 3.5.1 Large Synoptic Survey Telescope

The Large Synoptic Survey Telescope (LSST) is a ground-based observatory currently being constructed at an altitude of 2,682 metres on the mountain Cerro Pachón in central Chile. Largely privately funded, the observatory is being designed and constructed by organisations from the United States. The idea was proposed in 2001 and evolved from the concept of a dark matter telescope. The main purpose of the telescope is to perform a very large survey of the sky, from near earth objects to the furthest reaches of the Milky Way. The total area the survey will cover is around 18,000 square degrees, or 43% of the sky.

The main science goals of the observatory are:

- A comprehensive survey of the solar system. Objects which travel close enough to Earth with a diameter of over 140 m to be considered hazardous will be catalogued. Objects in the Kuiper belt and trans-Neptunian objects will be studied in great depth to better understand the evolution of the solar system.
- Study the structure and stellar content of the Milky Way. Through wide-field photometry, parallax, proper motion and spectroscopy, galactic formation and evolution can be better understood. This will also result in a highly accurate map of the galaxy.
- Study dark matter and dark energy. This is done through a combination of measuring weak gravitational lensing and photometry of supernovae as a function of redshift.
- Measuring faint variable and transient objects. These include neutron star and black hole binary systems and the optical components of gamma-ray bursts. Previous studies have been unable to detect these due to lack of field of view or sensitivity.

One of the hopes for the LSST is serendipitous, or accidental, discoveries. Due to the large field of view and sensitivity of the system and the massive amounts of data it will output, there is a real possibility of imaging something that has not been seen or predicted before.

The sensors being used for imaging are 189 CCD250s manufactured by e2v and STA/ITL, totalling 3.2 billion pixels. The arrangement of the focal plane array is shown in Figure 3-4 [20].

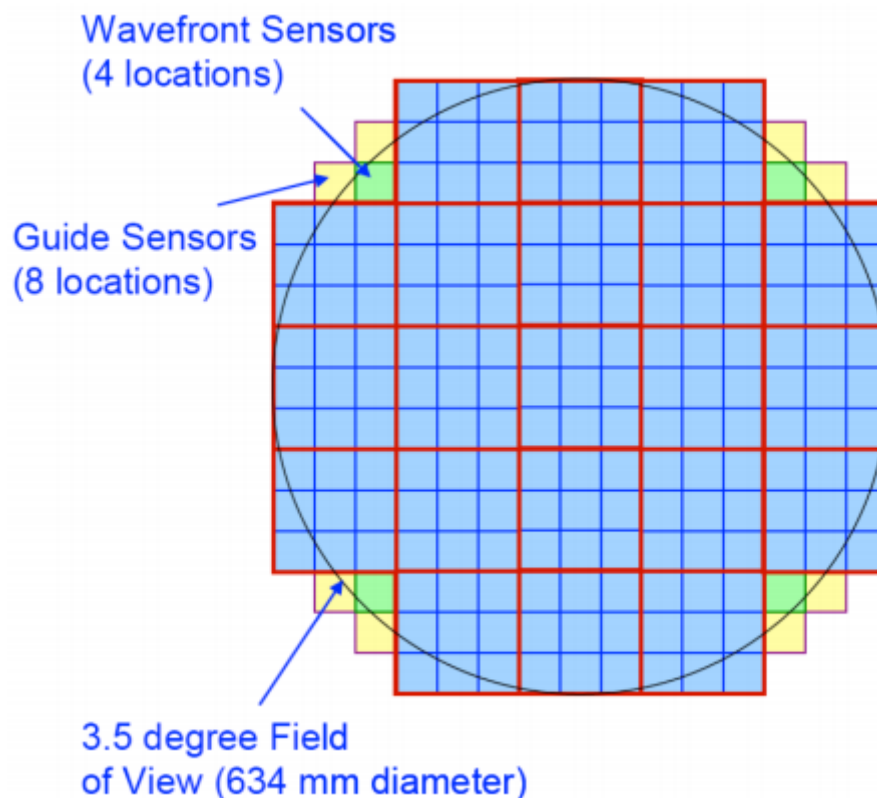


Figure 3-4: Focal plane array of the LSST.

Requirements of this camera were high quantum efficiency across the spectral range, a sensor with a small contribution to the point spread function and fast readout (< 2 seconds). Specifications are given in Table 3-4.

Characteristic	Value
Type	CCD250
Format	189 arrays of 4000 × 4000 pixels
Pixel Pitch	10 μm × 10 μm
Spectral Range	320 to 1080 nm
Number of outputs	16
Noise	5 e <sup>-</sup>
Dark Signal	1.02 e <sup>-</sup> /minute at 143 K
Quantum Efficiency	68 % @ 350 nm 89.4% @ 500 nm 95.2% @ 620 nm 98.4% @ 750 87.5% @ 850 29.9% @ 1000
Gain	0.69 e <sup>-</sup> /ADU
Full Well Capacity	144,000 e <sup>-</sup>

*Table 3-4: Metrics for the 189 CCDs in the focal array of LSST.*

### 3.5.2 Euclid

Euclid is a space telescope currently under development by ESA for detecting visible and near-infrared wavelengths. It is a medium-class mission and has a budget of around €500 million. It is designed to make advancements on the technology in ESA's own Planck telescope and the data from both will complement each other. It was chosen as a mission in 2011 with a speculated launch date of 2022. It will be sent into orbit at L2, where its mission will last at least 6 years. During its mission it will observe 15,000 square degrees of the sky. In addition to the wide field survey, there will be deeper observations in two areas of around 20 square degrees.

The science goals of the missions are:

- Map the distribution of dark energy. This is done by measuring the shape distortions of distant galaxies due to weak gravitational lensing from intermediate galaxies.



- Map the expansion of the universe. This will be done with coarse measurements of the red shift of over one billion galaxies. Of this one billion, millions of objects of interest will be measured at a much greater precision.

The measurements of photons in the visible wavelengths will be done with 36 CCD273s manufactured by e2v, specifically optimised for the Euclid mission. They are arranged in a 6 x 6 square pattern with minimal gaps between the sensors. The main constraints on the imager were that it must have a low point spread function to accurately reproduce the shapes of galaxies, it must be sensitive enough to image distant, faint objects and have low readout noise. Sensor characteristics are given in Table 3-5.

Characteristic	Value
Type	CCD273
Format	36 arrays of 4096 × 4132 pixels
Pixel Pitch	12 $\mu\text{m}$ × 12 $\mu\text{m}$
Spectral Range	550 to 900 nm
Noise	< 3.6 $\text{e}^-$
Dark Signal	< 1 $\text{e}^-/\text{pixel}/\text{minute}$ at 173 K
Quantum Efficiency	83% @ 550 nm 83% @ 750 23% @ 850
Gain	13.1 $\text{e}^-/\text{ADU}$
Full Well Capacity	> 175,000 $\text{e}^-$

*Table 3-5: Metrics for the 36 CCDs in the focal array of Euclid.*

### 3.5.3 TAOS II

The Trans-Neptunian Automated Occultation Survey [21] is a set of three ground-based telescopes located in Baja California, Mexico. They are situated at an elevation of 2,830 m in an area with typically clear skies, low humidity and very little light pollution. The observatory is a collaborative effort between Taiwan, the United States and Mexico designed to study small objects within the

solar system and further afield. The telescope installation begun in 2013, with completion scheduled for 2019, although data has yet to be released.

The main science goal for this observatory is to detect objects in the Kuiper belt and beyond. These objects are far too dim to be imaged directly, so their presence will be inferred from the occultation of over 10,000 stars. To do this, all of the stars are imaged continuously, and the brightness recorded. Any decrease in brightness indicates an occultation and thus an object passing between the telescope and the star. These occultations are very rare ( $< 10^{-3}$  per star per year) and have a very short duration ( $\approx 200$  ms), necessitating the large number of stars measured and also a high frame rate ( $\approx 20$  Hz). The use of three telescopes allows for the rejection of false positives as the occultation must be measured on all three to be considered a true event.

Due to the high framerate demands, CMOS sensors were chosen for the focal plane. At the readout speeds necessary, CCDs could not meet the low noise demands,  $< 5 \text{ e}^-$ . The use of CMOS also has the inherent advantages of selective readout. Using a region of  $6 \times 6$  pixels for each star, measuring a field of 20,000 stars will only use 1 % of the pixels in the array used in TAOS II. Being able to read just these pixels reduces the bandwidth requirements for readout and reduces readout noise and the volume of data.

The sensors used in TAOS II are CIS113 designed by e2v Technologies. Each of the three focal arrays contains ten sensors, butted on three sides, arranged as shown in Figure 3-5. The size and arrangement of the sensors allows for almost complete coverage of the focal plane, with only a small amount lost on the pinout sections. Specifications for the devices are shown in Table 3-6.

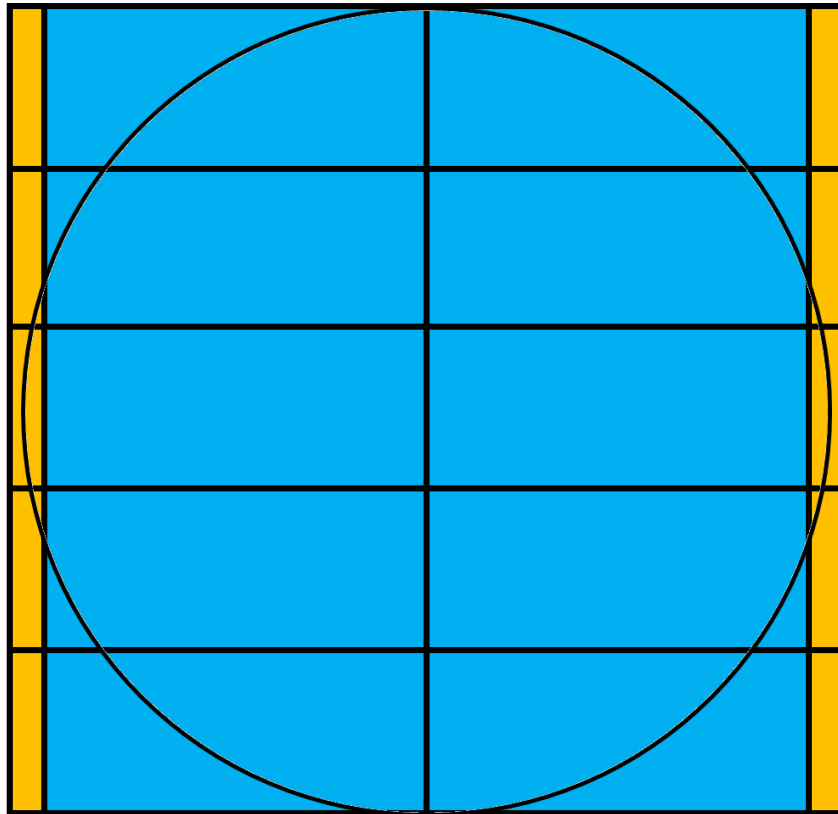


Figure 3-5: Focal plane array layout of one of the TAOS II telescopes. Blue areas indicate photosensitive area, orange the pinout regions for each device and the circle is the focal plane.

Characteristic	Value
Type	CMOS
Format	10 arrays of 1920 × 4608 pixels per telescope
Pixel Pitch	16 μm × 16 μm
Spectral Range	400 to 900 nm
Noise	< 2.3 e <sup>-</sup>
Dark Signal	< 9 e <sup>-</sup> /pixel/minute at 248 K
Quantum Efficiency	48% @ 400 nm 86% @ 600 nm 32% @ 900 nm
Gain	77.4 μV / e <sup>-</sup>
Full Well Capacity	> 16,100 e <sup>-</sup>

Table 3-6: Specifications of the CIS 113 devices installed in the TAOS II focal plane array.

### 3.5.4 GravityCam

GravityCam is a proposed ground-based sensor array that has been proposed to be installed on an existing telescope, the New Technology Telescope (NTT) located in the Atacama Desert, Chile. The NTT is located at an altitude of 2,375 m. Originally proposed in 2015, baseline studies are ongoing to determine the viability of the project.

The goal of the project is to provide wide-field, high resolution imaging and wide-field, high-speed photometry from a ground-based telescope. The use of lucky imaging will increase the resolution of the images 3-5 times that which is currently possible from the ground without the use of adaptive optics. With this increased resolution the project aims to:

- Increase the rate of detection of Earth sized planets through gravitational microlensing
- Conduct weak shear studies of dark matter distribution in distant galaxy clusters
- Obtain data for fast multiwavelength flaring in accreting objects
- Generate data on objects in the Kuiper belt and possibly the Oort cloud

A high readout rate, greater than 10 Hz, is needed for the measurements of events with a small timescale, but also to conduct lucky imaging. The imagers must all be capable of these framerates with full frame readout. The noise must also be kept very low to facilitate the imaging of faint objects. These two restrictions limit the choice of sensor to either a CMOS sensor or an EMCCD.

Both sensors can achieve high framerates with low noise values, but each have their own disadvantages. EMCCDs suffer from a very low fill factor when arranged in an array, due to the shielded region of the frame transfer device and the gain register. As little as 16% of a mosaic of EMCCDs is sensitive to light. CMOS sensors do not need any light shielding for their readout structures and so can achieve fill factors of over 85% of the field of view.

CMOS sensors operating at high framerates still suffer from readout noise which is too large to be negligible. The noise is also not uniform, which makes it difficult to account for when processing images. EMCCDs are capable of sub-electron noise and can even be used in photon counting mode.

The CMOS sensor under consideration for use in GravityCam is the CIS120 from Teledyne e2v, capable of 20 Hz readout rate, with on chip ADCs. The device is still in its early stages of development, with a small number of early revisions having been tested. The devices are promising, but still need refinement to reduce the readout noise, currently  $4 e^-$ . Any devices used would need extensive characterisation, which will increase the cost of the project. Reported characteristics are given in Table 3-7.

Characteristic	Value
Type	CMOS
Format	$2048 \times 2048$
Pixel Pitch	$10 \mu\text{m} \times 10 \mu\text{m}$
Spectral Range	400 to 900 nm
Noise	$4 e^-$
Dark Signal	$< 9 e^-/\text{pixel}/\text{minute}$ at 248 K
Quantum Efficiency	75% @ 400 nm 90% @ 600 nm 28% @ 900 nm
Gain	$40 \mu\text{V} / e^-$
Full Well Capacity	$35,000 e^-$

Table 3-7: Specifications of the CIS 120 currently under consideration for use in GravityCam.

The estimated costs of using these technologies is around ~€15 million if CMOS technology is used, and ~€10 million if EMCCDs are chosen [22]. Although the cost of CMOS is higher, it will allow for a five-fold increase in the data being obtained for only a 50 % increase in price.

### 3.6 Conclusions

In this chapter, a number of ground- and space-based observatories have been discussed. The science missions of each have been detailed, along with the sensor requirements to achieve these

goals. Detailed sensor characteristics have been presented to allow for direct comparison between them.

Although all of the past missions discussed in this chapter have utilised CCDs for their imaging arrays, the rapid development of CMOS sensors has increased their potential for use in precision astronomy, as is evidenced by the desire to use them in upcoming missions. The CMOS observatories discussed will act as test beds for future missions. If the results obtained are comparable to those of ground-based telescopes using CCDs, it will lead the way forward and accelerate their use in space, where their inherent radiation hardness will give them an advantage over CCDs.

### 3.7 References

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## 4 Baseline Sensor Characterisation

### 4.1 Introduction

As technology progresses, feature size in silicon sensors is reducing, leading to many advantages such as increased pixel density and fill factor. As the features shrink further, smaller defects may have an impact on performance, even down to the atomic level. These can include variations in the doping levels, purity of the silicon, thickness of metal tracks and the size of transistors. Two sensors made on the same wafer may have slight discrepancies in certain operational parameters that can lead to differences in the images they produce.

Since no sensor is exactly the same as another, it is important to know the exact details of how each one performs in the most fundamental metrics. As all of these metrics will have an impact on any image taken with the sensor, they must be studied in depth so that any effect they may have can be accounted for and removed, if possible, by image processing.

This section describes the theory of some of the metrics used to characterise a sensor as well as presenting and discussing the characterisation of the sensor. An in-depth description of the readout electronics, software and BSB1 sensors is also given.

### 4.2 Sensor Characterisation Theory

#### 4.2.1 Conversion Gain

When a sensor is read out, the number of electrons is indirectly measured as a voltage and the voltage converted into a digital number by an ADC. The conversion from the number of electrons to a voltage is done by the source follower and the sense node and is known as conversion gain, or Charge-to-Voltage Factor (CVF), in units  $V/e^-$ . A larger gain corresponds to a greater sensitivity, but usually at the cost of a reduced full well capacity. The system gain is the total gain of all of the readout electronics, including the conversion to Analogue Digital Units (ADUs). This is given in the units  $e^-/ADU$ . In general, the relationship between volts and digital numbers is known, and so to get



the system gain a technique known as the photon transfer curve is employed which is discussed later.

#### 4.2.2 Linearity

In an ideal sensor, the signal output is linearly proportional to the number of photons it has absorbed. In this case the gain remains constant at all signal levels. In real devices, as the signal begins to reach full well capacity, the gain begins to decrease to a point where this must be accounted for when measuring the brightness of objects. The cause of this is two-fold. Firstly, in CMOS devices the sense node capacitance is kept small to increase the CVF. This small capacitance is non-linear and changes as the amount of collected charge increases [1]. Since the output voltage is determined by the equation  $V = q/C$ , any change in capacitance changes the output voltage. The second cause is non-linearity in the source follower amplifier.

Linearity measurements are generally defined as a percentage variation, when compared with an ideal linear response, up to a percentage of full well capacity i.e. 5% nonlinearity up to 95% full well. This means the signal does not deviate from the expected signal by more than  $\pm 2.5\%$  up to 95% of the sensors full well capacity. CMOS sensors with calibration applied, in the form of correcting a characterised linearity curve, have achieved linearity of up to 99.94% to full well [2].

#### 4.2.3 Full Well Capacity

The full well capacity is a measure of how many electrons can be collected in a single integration period, and therefore how many photons can be measured. In general, the higher the full well capacity the better, as it directly impacts both the dynamic range of the sensor and the signal-to-noise ratio. The dynamic range is the ratio between the minimum and maximum achievable signals. High dynamic range makes distinguishing small variations in light easier as well as being able to image both bright and dark areas simultaneously. The signal-to-noise ratio is the ratio of signal and noise at a specific signal value. The full well capacity can be improved with larger pixels, a large floating diffusion capacity or by novel techniques such as multiple charge transfers per readout [3].

#### 4.2.4 Dark Current

Dark current arises due to the thermal generation of electrons in the sensor. It gets its name from the fact that these electrons are generated even when no light is incident upon the sensor. Charge generated in this manner is detrimental to imaging as it has no correlation to the number of photons collected during the integration period. The rate of electron generation is known as dark current, while the number of electrons measured is known as the dark signal. Sensor temperature and integration time do have an effect on the measured dark signal.

There are three main regions in which dark current is generated – the undepleted silicon, the depletion region within the photodiode and surface states at the silicon – silicon oxide (Si-SiO<sub>2</sub>) interface.

In the undepleted bulk silicon, electrons are present due to the dopant ions and will diffuse throughout the material due to the non-uniform concentration of carriers in the material. The number of electrons depends on the doping concentration. Any charges near the edge of the depletion region have a chance of diffusing into the depleted space-charge and will be moved into the potential well. The dark current from diffusion  $J_s$  proportional to the temperature  $T$  is given as

$$J_s \propto T^{3+\gamma/2} \exp\left(-\frac{E_g}{kT}\right) \quad (4-1)$$

Where,  $\gamma$  is a constant related to electron diffusion and carrier time,  $E_g$  is the band gap and  $k$  is Boltzmann's constant.

Dark signal electrons in the depletion region are generated through the Shockley-Read-Hall generation-recombination mechanism [4]. Impurities in the silicon lattice, known as traps, allow energy levels within the bandgap, which act as steps for electrons to transition from the valence to conduction band. Since the electrons generated in the depletion region are already within the field, all of them will be captured in the potential well and will thus be read out as dark signal in the

image. As there is a deficit of carriers in the depletion region, generation will dominate. Dark current from generation within the depletion region  $J_{gen}$  is given as

$$J_{gen} = \frac{qn_iW}{\tau_e} \quad (4-2)$$

Where  $q$  is the charge of an electron,  $n_i$  is the intrinsic carrier density,  $W$  is the channel width and  $\tau_e$  is the effective lifetime.

The generation is shown to have a similar temperature dependence as  $n_i$  [5], which is given by

$$n_i = M T^{3/2} \exp\left(-\frac{E_g}{2kT}\right) \quad (4-3)$$

Where  $M$  is a constant related to the density-of-state effective mass of electrons, the valence band, and the number of equivalent minima in the conduction band. The density-of-state effective mass is the effective mass derived from the density of states in a parabolic conduction band [6].

From Equations (4-1) and (4-3) it can be seen that the dark current is exponentially dependent upon the operating temperature of the device. Any device being used should therefore be cooled during operation in order to minimise the dark signal.

The Si-SiO<sub>2</sub> interface is the dominant source of dark signal in all sensors. This is due to the molecular structure of the bonds formed at the interface. The silicon dioxide crystal structure is much larger than that of standard silicon, and so the lattices do not align, shown in Figure 4-1.

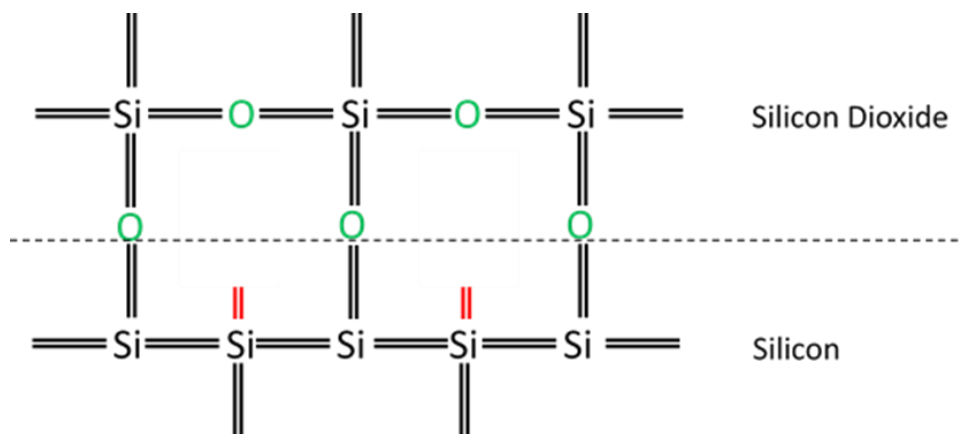


Figure 4-1: Difference in lattice sizes of silicon and silicon dioxide. Dangling bonds are shown in red.

In the areas where the two lattices do not align properly, some of the silicon bonds are left unformed, known as “dangling bonds”. These act in a similar fashion to defects within the crystal lattice, giving step in the middle of the band gap, making it easier for electrons to reach the conduction band. These dangling bonds can be passivated with the introduction of atomic hydrogen, decreasing the rate of dark signal generation [7], however this may not passivate all bonds and some may still exist.

Although the rate of generation of dark signal due to this interface is still dependent upon temperature, the most effective way of reducing its affect is by moving the charge collection region away from the surface as in a buried channel device. This brings the potential well away from the surface of the device, preventing the interaction with dangling bonds, thus removing the source of dark current.

For all measurements taken in this thesis, the devices were run at room temperature, 296 K, with the same frame rate. This means that the dark current generated will be the same throughout. To remove the effects of dark current, at the start of each test run 100 dark images are taken and the mean signal found. This mean signal is then subtracted from the subsequent images.

#### 4.2.5 Quantum Efficiency

Quantum efficiency is a measure of how sensitive a sensor is to a particular wavelength of light and is usually quoted as a percentage. It describes the fraction photons at that wavelength that are likely to interact with the silicon and generate a signal electron.

Quantum efficiency varies greatly with wavelength due to the absorption depth and reflection of the photons. For wavelengths below 400 nm, a large proportion of light is reflected from the surface of silicon and cannot be readily measured. For wavelengths longer than this, the absorption depth increases with wavelength. At 500 nm the absorption depth is  $\sim 1 \mu\text{m}$ , meaning that after  $1 \mu\text{m}$  only 36% ( $1/e$ ) of photons remain unabsorbed. At this wavelength, the quantum efficiency is usually high because most sensors are far thicker than the absorption depth. For a photon of wavelength 1000

nm, the absorption depth is  $\sim 100\text{ }\mu\text{m}$ . Most CMOS devices manufactured are thinned to much lower thicknesses than this, so a large majority of photons pass through the sensor without interacting. This leads to much lower values for quantum efficiency at 1000 nm.

Anti-reflective coatings can be added to sensors to increase the quantum efficiency at short wavelengths by decreasing the proportion of light reflected by the surface of the device [8]. To remedy a low quantum efficiency at long wavelengths, a CMOS device can be made thicker to increase the chance of photon interaction. This however leads to another problem discussed in the next section.

#### 4.2.6 Charge Spreading

Since shorter wavelengths are absorbed at much smaller depths than longer wavelengths, electrons are generated near the surface of the device. If the device is illuminated from the back side, this means that the electrons are generated on the opposite side to the photodiode. Since standard CMOS image sensors are not capable of full depletion, this leads to the electrons being generated in the field free region, shown in Figure 4-2. These electrons can then diffuse freely through the field free region in random directions until they encounter an electric field, at which point they will be captured. If this field is in a different pixel to the one in which the electron was generated, this will result in charge spreading, shown by the black dotted line. Longer wavelengths are more likely to penetrate deep enough to generate an electron within the electric field. A spreading of charge can lead to shape distortions in images and increase the perceived size of point sources such as stars.

Charge spreading will be discussed in further detail in Chapter 6.

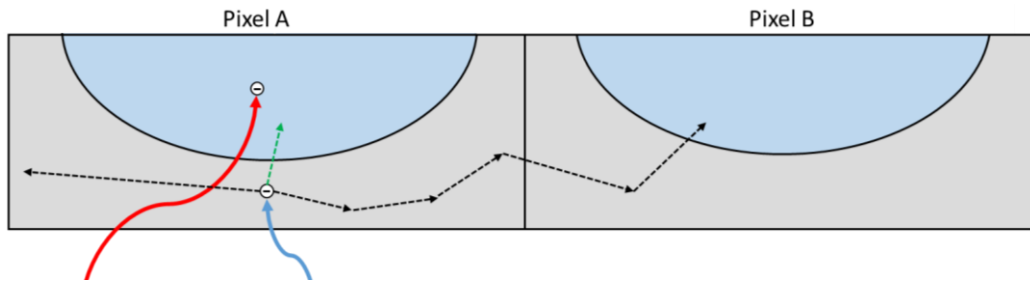


Figure 4-2: Simplified representation of charge spreading between two pixels. The blue line represents a shorter wavelength and the red represents a longer wavelength. The blue areas represent the electric field within each pixel. The green line shows when an electron is captured by the correct pixel, and black lines show its random walk to other pixels.

#### 4.2.7 Image Lag

Image lag arises due to the incomplete transfer of electrons in the readout period. This can result in not only electrons not being measured in that frame, but they may also be read out in the subsequent frame. This can lead to image ghosting, where some objects imaged in the previous frame are visible in the next frame. Image lag is discussed in much greater detail in Chapter 5.

#### 4.2.8 Photon Transfer Curve

The photon transfer curve (PTC) is a powerful characterisation technique which can be used to determine many of the metrics mentioned in the previous sections and optimise camera performance. It can be a very quick way to verify that a system is working properly, or to diagnose any issues it may have. The curve plots the noise in the images generated by the sensor versus with the signal level in the image. The characteristic shape of a PTC is shown in Figure 4-3.

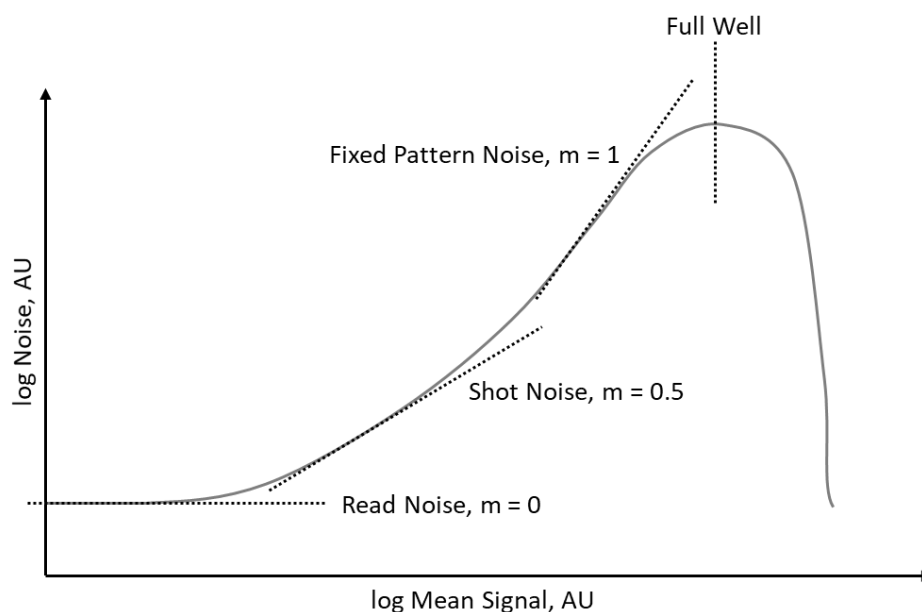


Figure 4-3: An ideal photon transfer curve showing the read noise floor, shot noise, fixed pattern noise and the full well capacity. The axes are in arbitrary units.

The first portion of the graph shows the read noise floor of the system, where the gradient,  $m$ , is equal to zero. In this section, the noise is dominated by sources in the readout electronics and it represents the lowest value for noise that the sensor can attain.

Once the noise floor is surpassed, the graph becomes dominated by shot noise. Shot noise arises from the random nature of the arrival of photons. Photons are subject to Poisson statistics, and so the noise is proportional to the square root of the signal, hence the gradient  $m = 0.5$ .

At higher signals, the images become dominated by fixed pattern noise, caused by non-uniformity between the pixels in the sensor, with each pixel giving slightly different signal levels to the rest even under equal light levels. These non-uniformities arise from slight inconsistencies in manufacture, and so are present in all images. The effect of these discrepancies can be minimised through frame subtraction, although this does increase the shot noise by a factor of  $\sqrt{2}$ . The fixed pattern noise is proportional to the signal, giving the gradient  $m = 1$  in the graph. The effects of fixed pattern noise are removed in astronomical images by dividing the raw image frames by a flat field frame – an image taken with all pixels under uniform illumination – thus normalising the signal. The normalised frame can then be multiplied by the average pixel value in the raw frame to generate an image frame with the fixed pattern noise removed.

The full capacity of the sensor can be seen in Figure 4-3 at the point where the noise is at its maximum. At this point, some of the pixels have reached the full well capacity and so will not collect any more charge. As the signal increases and the number of pixels at saturation rises, the noise begins to drop because the signal from the pixels are all approaching the same value. Once the sensor is fully saturated and all pixels are at full well capacity, the noise becomes zero.

To calculate gain, the graph may be plotted on linear axes and the gradient in the shot noise dominated portion found. The inverse of this gradient is equal to the system gain,  $K$  ( $e^-/ADU$ ), and is derived as follows [9]:

$$S = \frac{1}{K}N \quad (4-4)$$

where  $S$  is the signal in ADU and  $N$  is equal to the number of electrons in the pixel. Adding readout noise  $\sigma_R$ , the signal variance  $\sigma_S^2$ , is found through the propagation of errors:

$$\sigma_S^2 = \left(\frac{\partial S}{\partial N}\right)^2 \sigma_N^2 + \left(\frac{\partial S}{\partial K}\right)^2 \sigma_K^2 + \sigma_R^2 \quad (4-5)$$

Since  $K$  is a constant,  $\sigma_K^2 = 0$  and  $\sigma_N^2 = N$  from Poisson statistics, we can use (4-4) to get

$$K = \frac{S}{\sigma_S^2 - \sigma_R^2} \quad (4-6)$$

Since we are using the shot noise dominated region of the graph, we can assume that  $\sigma_S^2 \gg \sigma_R^2$ , leaving:

$$K = \frac{S}{\sigma_S^2} \quad (4-7)$$

The right-hand side of (4-7) is the inverse of the gradient of a straight line fitted to the graph.

As the gain, and all other parameters relevant to this thesis, can be inferred easily from a PTC with linear axes, this is the form in which they will be presented henceforth.

### 4.3 Device Details

#### 4.3.1 Sensors

The sensors used in this thesis are all novel devices designed within the CEI at the Open University [10]. The aim of these devices was to allow full depletion of a monolithic 4T CMOS sensor utilising pinned photodiodes at greater thicknesses than conventional sensors. A standard 4T CMOS device generally has a pinning voltage of less than 2 V, and thus a small depletion depth. This cannot be increased with reverse bias due to the p-wells containing the readout electronics. These p-wells are connected to the p<sup>+</sup> pinning implant, as well as the p<sup>-</sup> type epitaxial layer, which connects to the p<sup>++</sup> type layer on the back side where reverse bias would be applied. This leads to a resistive path being



formed to the p-wells, shown in Figure 4-4, which are held at ground, allowing a large leakage current through the device which would cause unwanted heat generation and damage to the sensor.

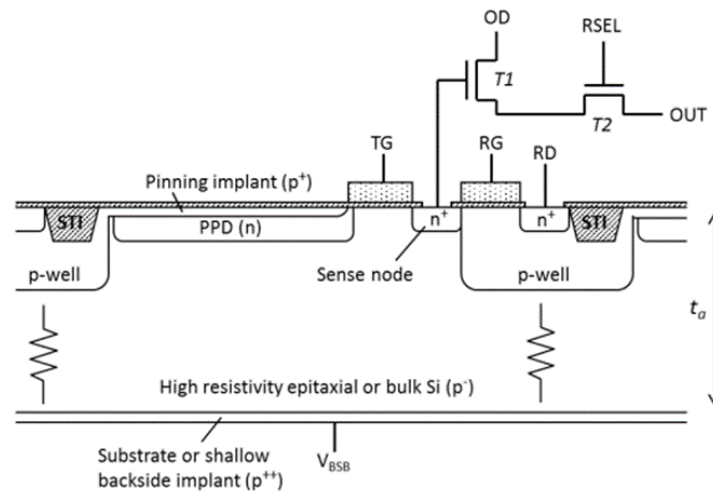


Figure 4-4: Resistive path formed through the p-wells,  $p^-$  epitaxial layer and back side  $p^+$  implant allowing current flow [9].

The design of these new sensors allows for reverse bias to be applied without inducing any leakage current. The reverse bias permits the device to be fully or even over depleted, decreasing charge spreading from short wavelength light. It also makes much thicker CMOS devices achievable, increasing the quantum efficiency at longer wavelengths.

Pinch-off is achieved by overlapping the depletion regions of adjacent pixels under the p-wells and thus interrupt the resistive path between the front and back faces of the device. To do this, an extra n-type implant, named the “Deep Depletion Extension” (DDE), is inserted beneath the p-wells, leaving the rest of the pixel unchanged. The entire pixel structure is shown in Figure 4-5.

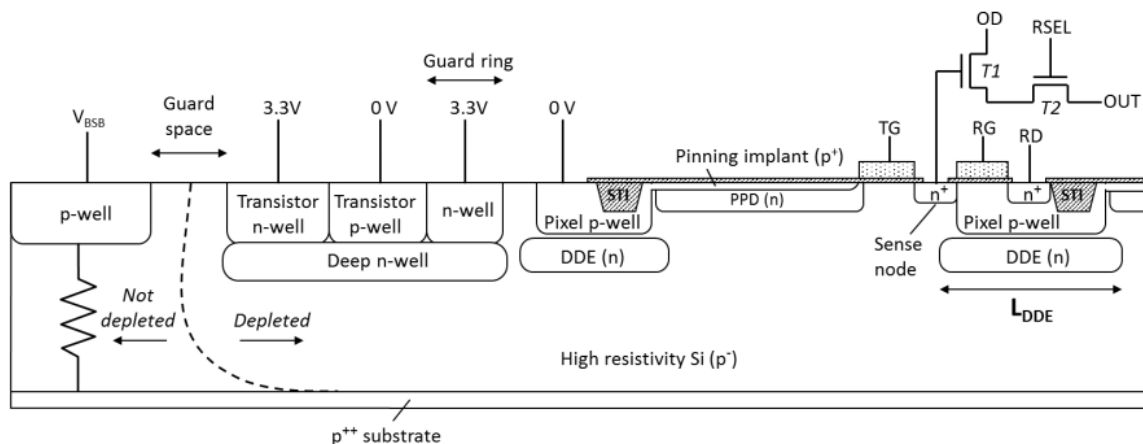


Figure 4-5: Pixel schematic of the new devices showing the DDE located under each p-well [9].

Under normal operating conditions, this implant becomes depleted and connects the depletion regions of neighbouring pixels. Simulation work was performed to ensure the DDE was designed in a way that made it less attractive to electrons than the photodiode so as not to interfere with charge collection.

The resulting sensors are known as Back Side Bias CMOS, or BSB1. Manufactured by TowerJazz, on 1000  $\Omega\text{cm}$ , 18  $\mu\text{m}$  thick silicon. Each chip contains eight  $32 \times 20$  pixel arrays, four of which are 10  $\mu\text{m}$  square, and the remaining four 5.4  $\mu\text{m}$ . Each of the four arrays of equal pixel size have varying DDE implants, with increasing overlap of the p-well.

Each sensor was designed with slightly different shape of the DDE implant and pinning voltage. One chip was manufactured with the same design parameters but no implant to act as a control device for comparison with the modified versions. The design variants are shown in Table 4-1.

DDE Implant dose	Low Vpin (1.5-1.6V)	High Vpin (1.7-1.8V)
None	-	W1-1
Low	-	W3-1
Middle	W7-1	W5-1, W5-2 & W6-2
High	W11-1	W9-1

Table 4-1: Design variants of the BSB1 devices. Device W5-2 is identical to W5-1 in design and was used after W5-1 failed.

The sensors are 18  $\mu\text{m}$  thick and front side illuminated apart from W6-2, which is a back-side illuminated variant of W5-2 back thinned to 12  $\mu\text{m}$ .

#### 4.3.2 Readout Control

Electronic control of the devices is done through LabView [11]. Rows are selected via the Graphical User Interface (GUI) timing diagram in a binary fashion, shown in Figure 4-6, which is sent to a National Instruments PXIe – 1073 with PXI-7852R card containing an FPGA, shown in the block diagram in Figure 4-7. This sends a signal to the row address to select a row to read out. The array to be read out is controlled in a similar fashion. Control over the transfer and reset transistors as well

as an LED are found in the timing diagram as well. The voltages to be applied are set manually before readings are taken. A timing diagram showing when signals are applied is shown in Figure 4-8 .

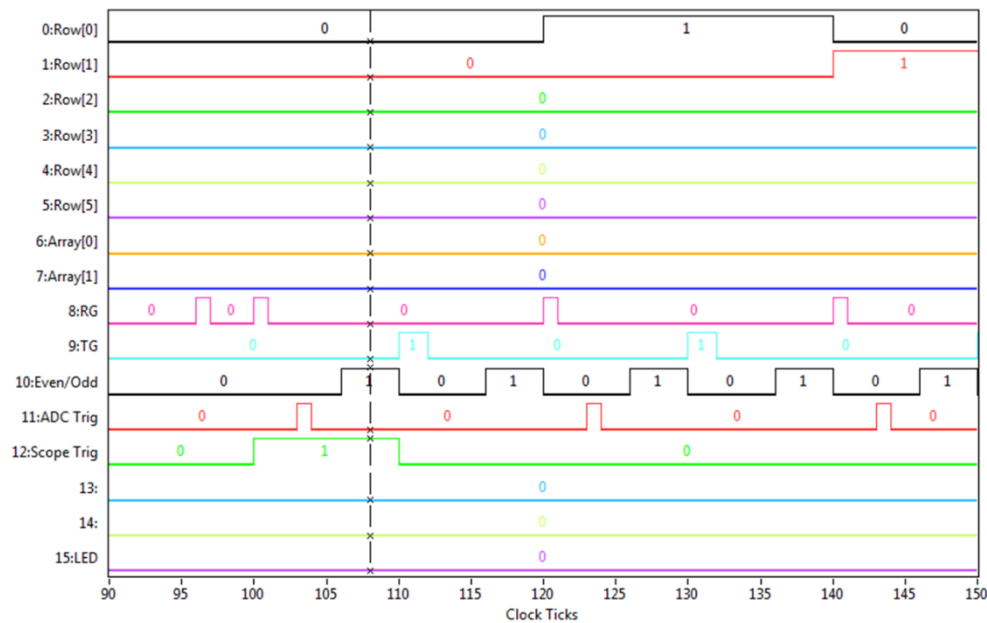


Figure 4-6: Graphical user interface used to control the timings of signals sent to the chip during charge transfer and readout phases.

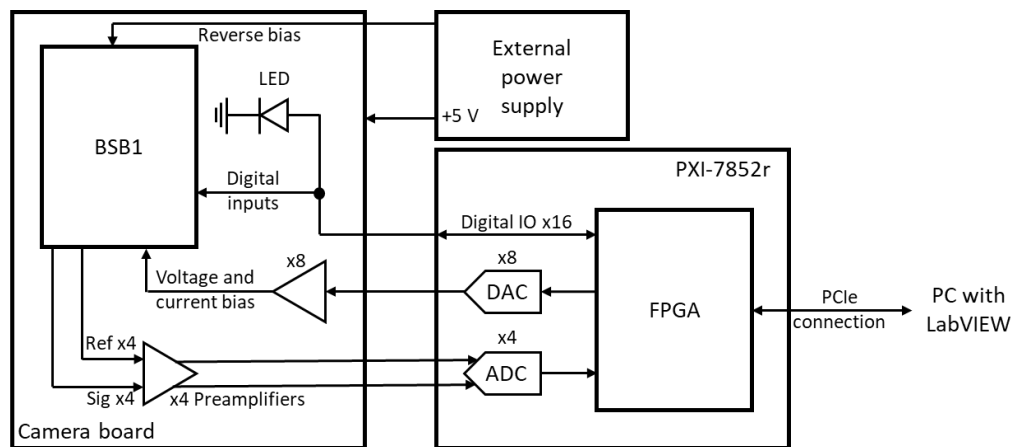


Figure 4-7: Block diagram of the power and data system used to control and read the BSB1 devices.

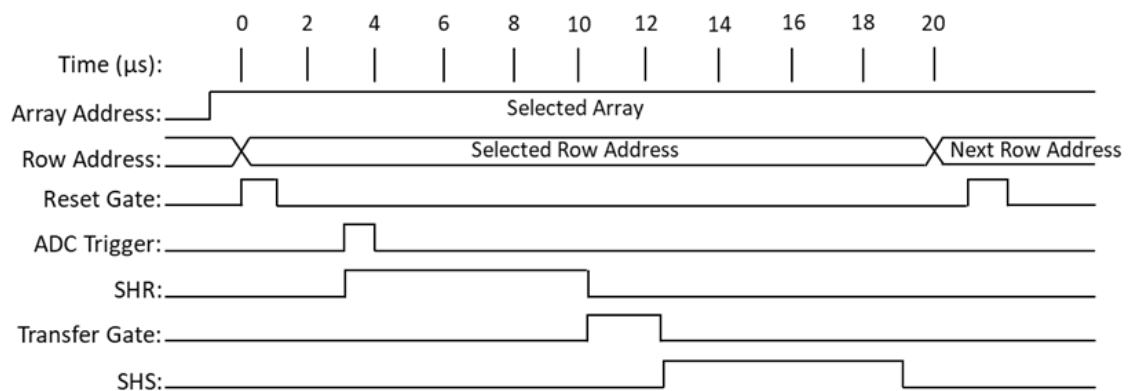


Figure 4-8: Timing diagram of signals used to read out a row of pixels.

Figure 4-9 shows a photograph of a BSB1 sensor mounted via a Zero Insertion Force (ZIF) socket to the Printed Circuit Board (PCB). All of the arrays' outputs are multiplexed to a single set of sixteen column source followers, meaning only the middle 16 columns are read. The outputs of the column source followers are then amplified and demultiplexed. The signals are then sent to the FPGA card, where digital CDS is applied to remove the reset noise and the voltage converted to a digital number by an ADC. The ADC has a bit depth of 16 bits and a maximum voltage swing of 20 V, giving a conversion of  $1 \text{ ADU} = 305 \mu\text{V}$ .

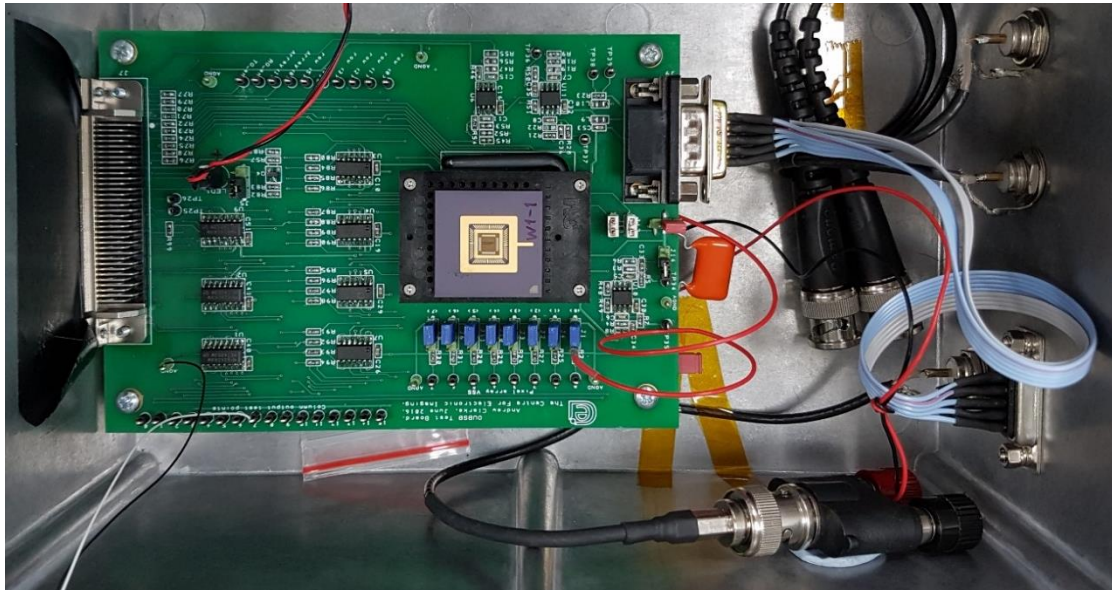


Figure 4-9: Photograph of a BSB1 device mounted on the PCB with connectors to external power source and data transmission lines.

The large connector on the left-hand side is to the National Instruments' card, which provides digital signals to the chip and reads the analogue outputs. The connector on the right supplies the analogue voltages to the board for both amplification and reverse bias.

Each of the pixel arrays is designed with a separate connection to the substrate. These are connected to individual pins, with test points on the board for measuring the leakage current.

#### 4.4 Characterisation Results

All results presented in this section are taken at room temperature at 10 frames per second and with biases listed in Table 4-2, apart from where stated.

Bias Name	Bias Voltage (V)
Reference Voltage ( $V_{OD}$ )	3.3
Floating Diffusion Reset Voltage ( $V_{DD}$ )	3.3
Reset Transistor Gate Voltage ( $V_{RG}$ )	3.3
Transfer Gate Voltage ( $V_{TG}$ )	3.3

Table 4-2: Biases used to drive the sensor during characterisation tests.

#### 4.4.1 Leakage Current

The purpose of these devices is to remove the substrate leakage current caused by the application of a reverse bias, so it is important to verify this. This was done by having the device continually taking images under normal conditions in darkness. The reverse bias is then slowly increased whilst the current is measured on external test points on the PCB. Results are shown in Figure 4-10.

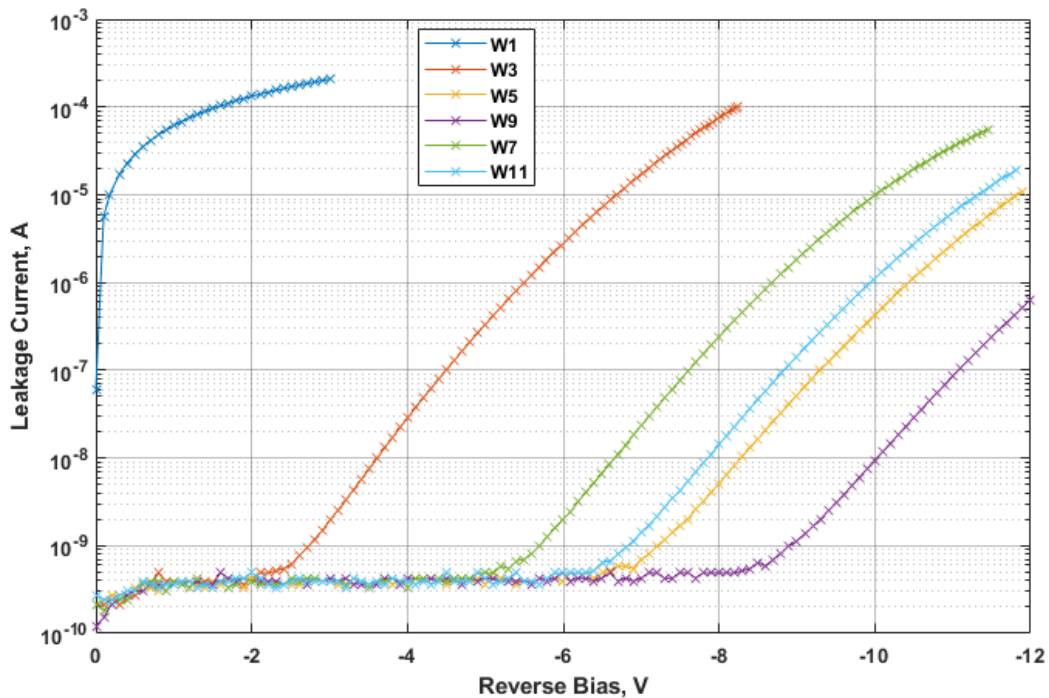


Figure 4-10: Measured reverse current with applied reverse bias voltage.

The results show that the DDE does indeed reduce the leakage current when reverse bias is applied.

W9 can have the largest reverse bias applied, which is expected as it has both the high pinning voltage and the largest DDE implant. W1, the control chip with no implant, exhibits a large current with very little reverse bias, demonstrating the need for the DDE.

These results show not only that the DDE implant is working as intended, but also gives the maximum operating voltage for the reverse bias that the chips can withstand.

#### 4.4.2 Photon Transfer Curves

Photon transfer measurements are taken by changing the period of time the LED is on during the integration time, which is kept constant. This method generates a photon transfer curve quicker than increasing the integration time, and also means the same dark current offset can be subtracted from all the images.

Initial tests are run on each of the sensors, from 0 V reverse bias to the maximum voltage they can tolerate. This is done to examine the effects the new implant and reverse bias may have on the electro-optical characteristics of the sensor. Each sensor is tested on all four arrays of 10  $\mu\text{m}$  pixels, however, only results for Array 0 and Array 3 are shown here as they are the two extremes of the implant.

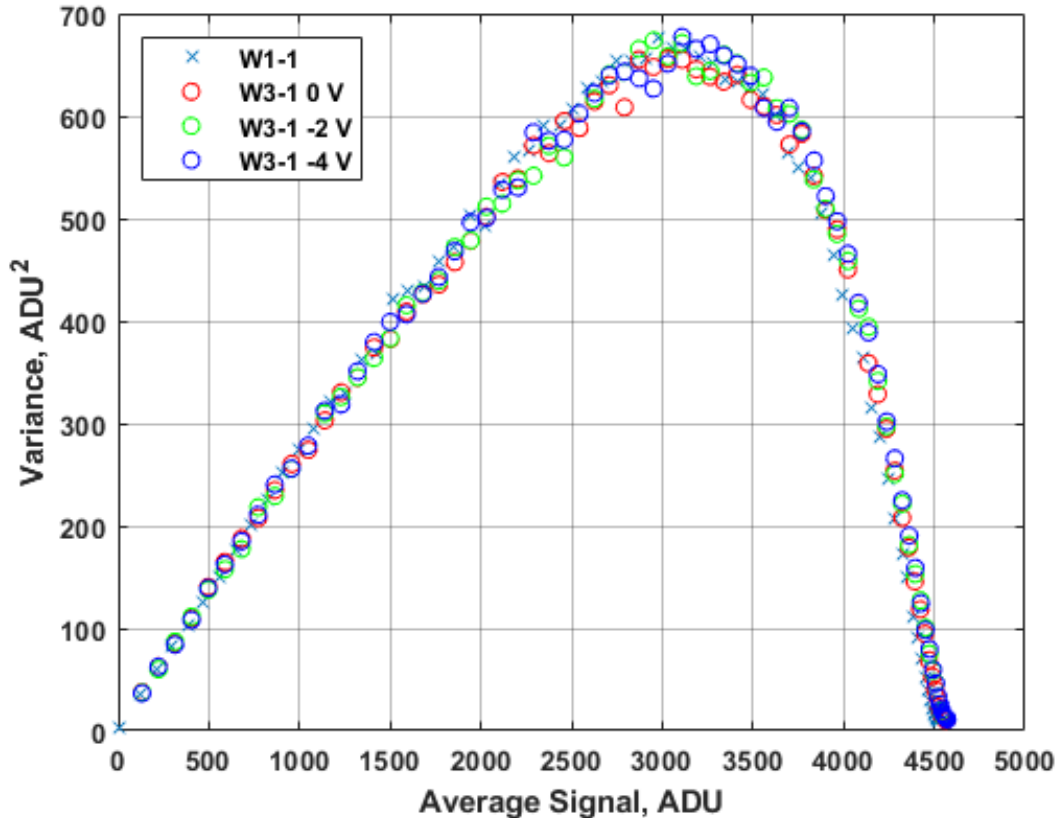


Figure 4-11: PTC from W3-1 Array 0 with no reverse bias, medium reverse bias and maximum reverse bias. W1-1 is shown as a comparison

Figure 4-11 shows the PTCs obtained from Array 0 of W3-1 with varying reverse biases. From the graph it can be seen that the reverse bias has negligible effect on the results, with the full well capacity remaining the same (3000 ADU) and the gain constant throughout. All of the devices show this behaviour on Array 0, indicating the small overlap has very little effect on the electro-optical characteristics of the sensors.

Using the first portion of the graph, where the variance is shot noise dominated, the gain of the device can be calculated.

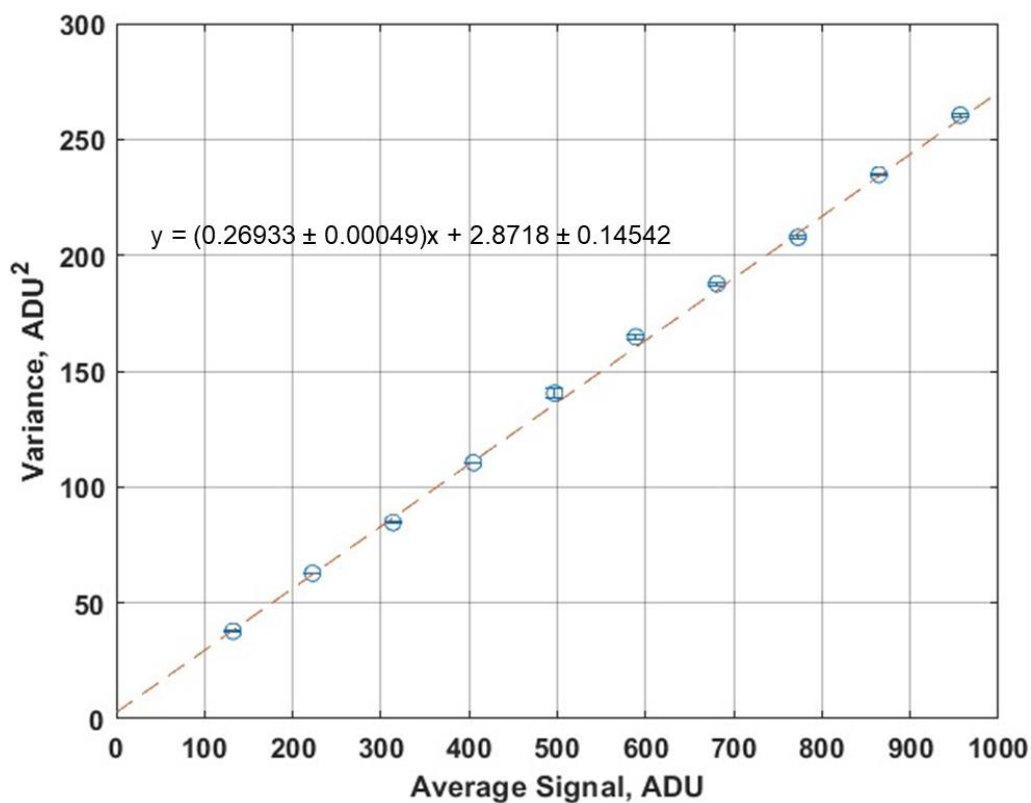


Figure 4-12: Portion of a gain curve taken from the previous PTC of W3-1 at 0 V reverse bias, with statistical uncertainty (standard deviation) included. The equation for the line of best fit is shown.

Figure 4-12 shows a segment of the PTC taken on Array 0 of W3-1 at 0 V reverse bias. A linear fit has been applied and has given the gradient as  $m = 0.26933 \pm 0.00049$ . From the theory given in Equation (4-7), the gain is equal to the inverse of this, giving a gain value of  $3.713 \pm 0.007 \text{ e}^-/\text{ADU}$ . We know that the ADC has a conversion of  $1 \text{ ADU} = 305 \text{ } \mu\text{V}$ , so we calculate that the CVF of the sensor is  $82.144 \pm 0.155 \text{ } \mu\text{V}/\text{e}^-$ . At -4 V, W3-1 has a gain of  $3.732 \pm 0.006 \text{ e}^-/\text{ADU}$ , a slight increase from 0 V reverse bias.

W1-1 was found to have a gain of  $3.723 \pm 0.004$  e<sup>-</sup>/ADU, a change of 0.3% which is well within error for most applications.

The gain of Array 0 for each device is calculated and shown in Table 4-3.

Device Name	Gain at 0 V (e <sup>-</sup> /ADU)	Gain at maximum reverse bias (e <sup>-</sup> /ADU)
W1-1	$3.723 \pm 0.004$	$3.723 \pm 0.004$
W3-1	$3.713 \pm 0.007$	$3.732 \pm 0.006$
W5-1	$3.897 \pm 0.011$	$3.846 \pm 0.005$
W7-1	$3.705 \pm 0.002$	$3.789 \pm 0.004$
W9-1	$3.766 \pm 0.005$	$3.798 \pm 0.008$
W11-1	$3.785 \pm 0.005$	$3.780 \pm 0.004$

*Table 4-3: Measured gain with uncertainty in Array 0 for every device. Gain is calculated at 0 V reverse bias and at the maximum reverse bias voltage the chip can sustain.*

The gain values vary slightly from device to device but remain fairly constant with the largest difference only 5% between W7-1 and W5-1. This is most likely due to manufacturing inconsistencies to do with the floating diffusion as they contain the same implant and only vary with pinning voltage. The majority of gain values are not within uncertainty range of one another indicating a genuine change in gain rather than variation due to systematic uncertainties.

The PTCs generated from Array 3 are largely similar to those of Array 0. Results from W3-1 Array 3 are shown in Figure 4-13. Again, the PTC follows that of W1-1 very closely with very little deviation, as do the PTCs for W5-1.

The rest of the devices show unusual behaviour in the PTCs for Array 3. Figure 4-14 shows the PTCs for W7-1 at various voltages. Although the full well capacity remains unchanged, there is a noticeable drop in variance as full well is approached when there is no reverse bias applied. However, once reverse bias is applied, the variance recovers, and the PTC returns to the shape close to that of W1-1.



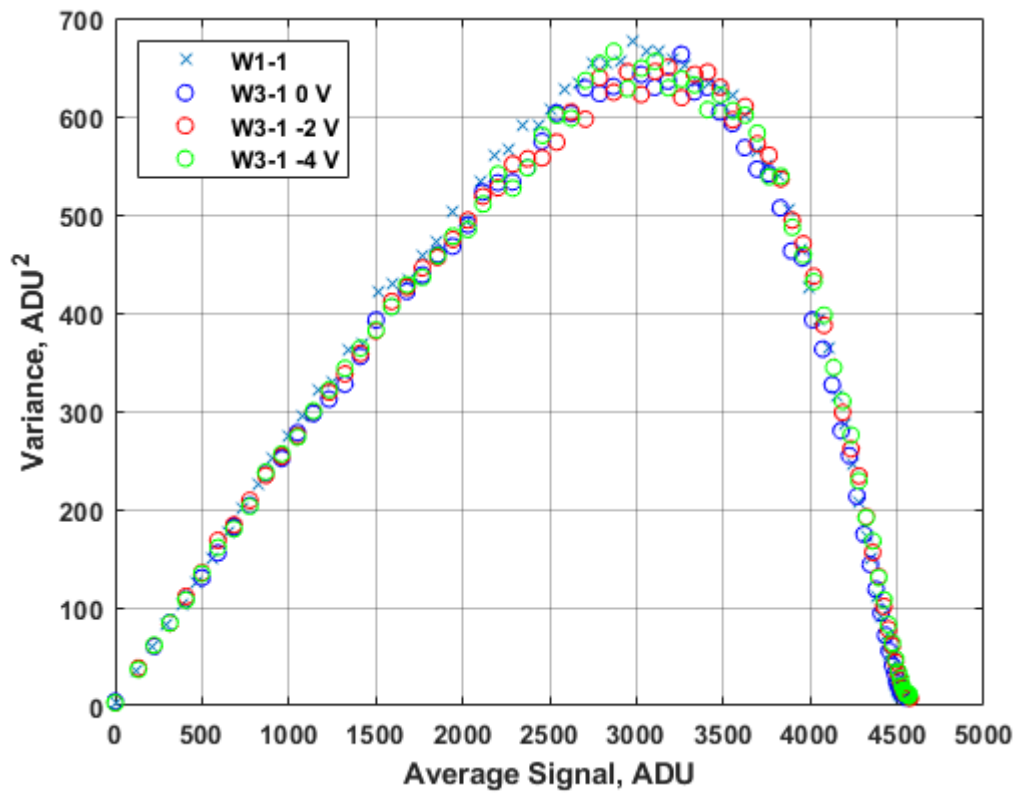


Figure 4-13: PTC from W3-1 Array 3 with no reverse bias, medium reverse bias and maximum reverse bias. W1-1 is shown as a comparison

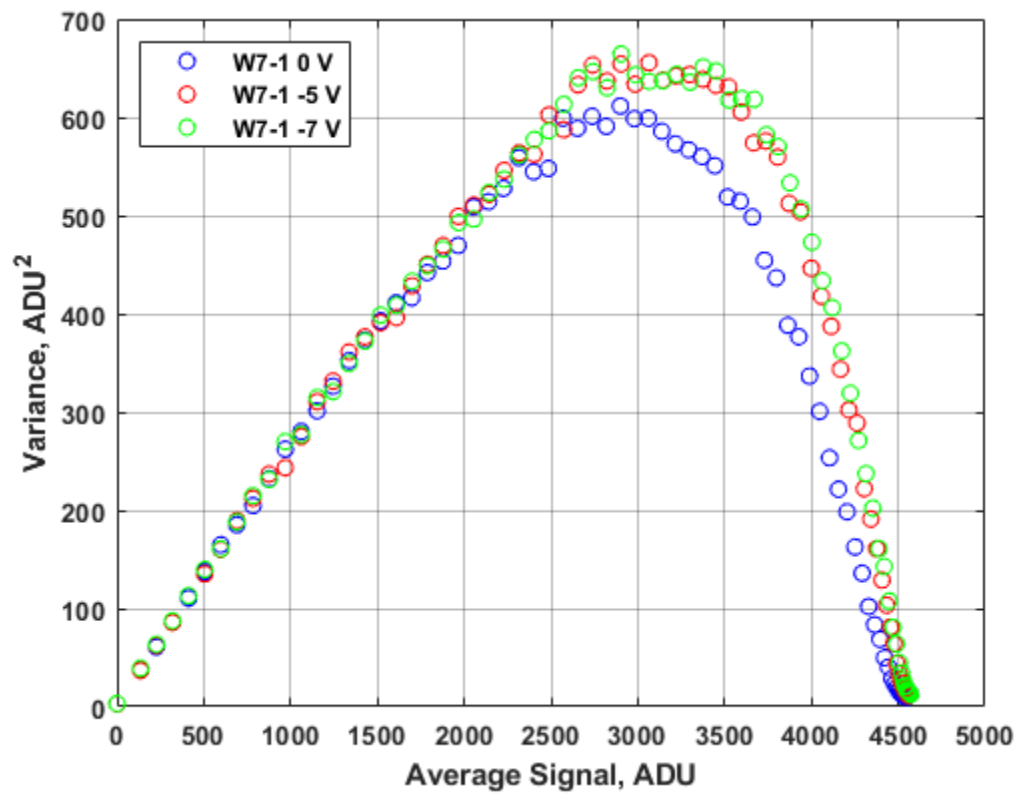


Figure 4-14: PTCs from W7-1 Array 3 with no reverse bias, medium reverse bias and maximum reverse bias.

A similar trend occurs in both W9-1 and W11-1, but to an even greater extent. In both cases, the full well capacity is decreases although the gain remains the same. These changes are shown in Figure 4-15 and Figure 4-16.

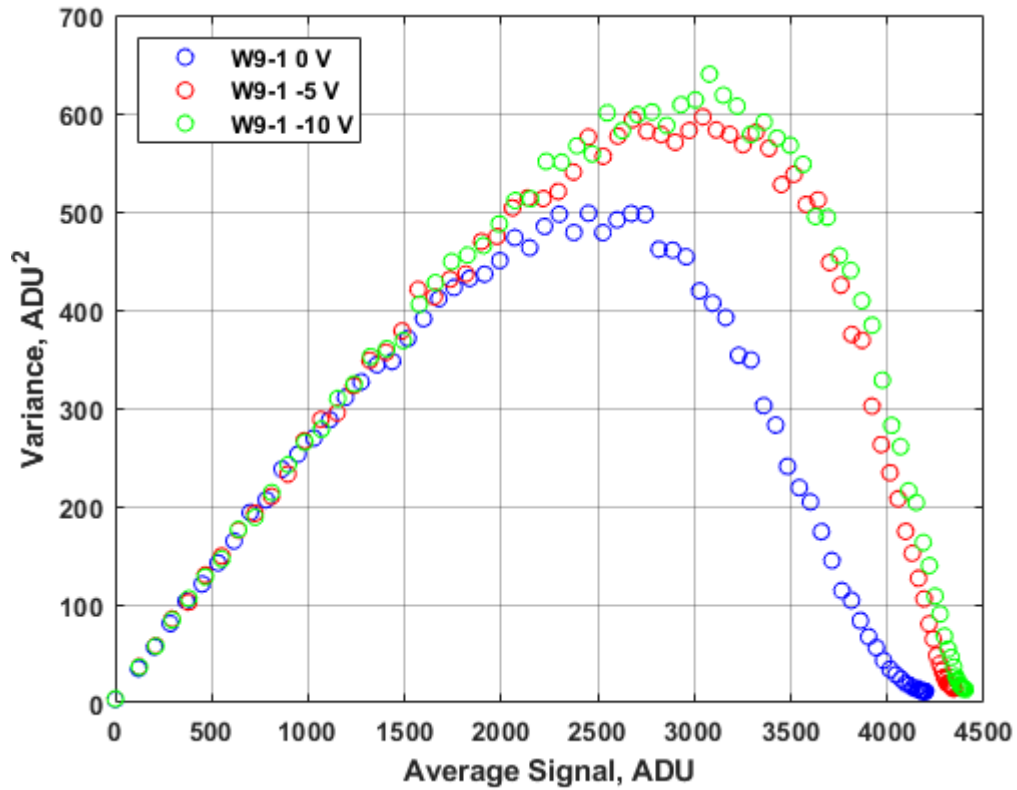


Figure 4-15: PTCs from W9-1 Array 3 with no reverse bias, medium reverse bias and maximum reverse bias.

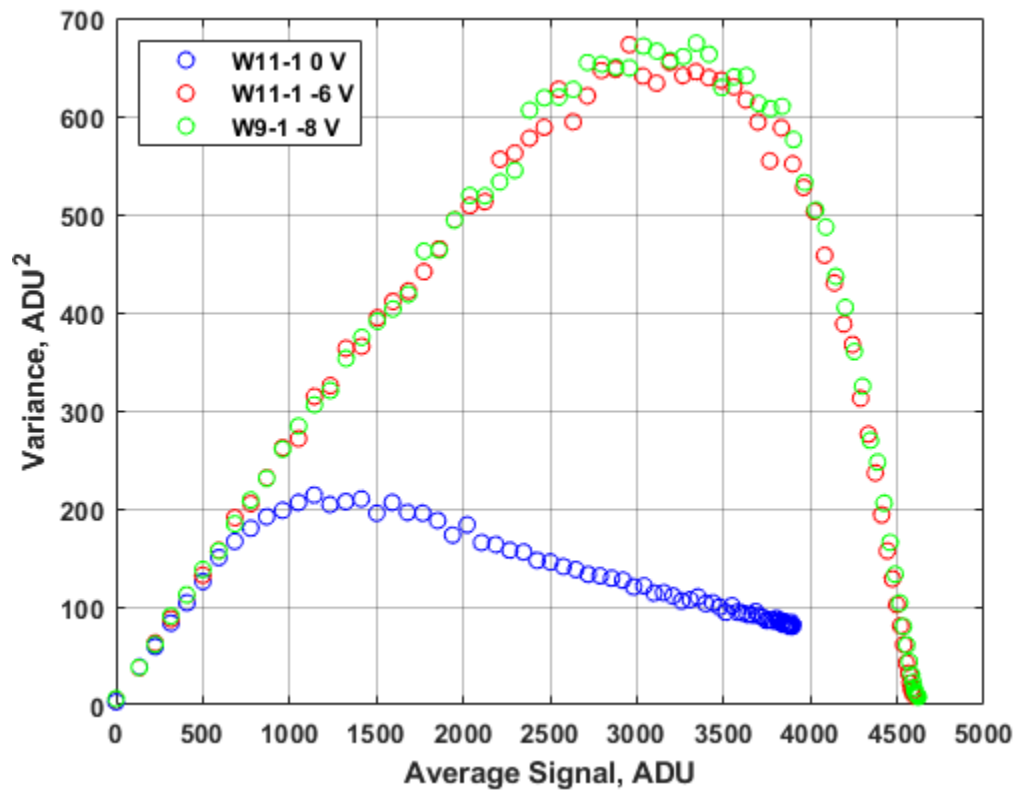


Figure 4-16: PTCs from W11-1 Array 3 with no reverse bias, medium reverse bias and maximum reverse bias.

As with W7-1, when no reverse bias is applied to both W9-1 and W11-1 the PTC has a greatly altered shape. Since the gain remains constant through all reverse biases, there is some form of charge loss occurring. This is caused by parasitic charge sharing between pixels. When the electrostatic potential within the DDE is more positive than that of the surrounding silicon, it forms a potential pocket in which electrons will collect. Due to the structure of the mesh structure of the DDE, electrons can move to the surrounding pixels until they reach the  $n^+$  guard ring at the edge of the array, where they will drain away. The application of reverse bias lowers the potential in the DDE, preventing the sharing of charge.

## 4.5 Linearity

Measuring the linearity of the devices is performed on the same images as the PTCs, but we are plotting the average signal in the device as a function of the illumination time during the integration period. A linear line of best fit is added to the straight portion of the graph, in this thesis between the second and twenty-fifth datapoint, and the equation of the line found. For each data point, the x-value is used in the equation, and the difference in y-values for the real data and the trendline is calculated. The difference is then divided by the y-value from the data and multiplied by 100 to give the percentage deviation from the trendline. These percentage deviations are then plotted against the signal to find where linearity falls outside of the 5% threshold. Measurements are done at multiple reverse biases to examine the impact.

Figure 4-17 shows the signal plotted against the time that the LED is on for, along with the linear trend line in yellow and its equation. This gives the values for calculating the residual. Signal is left in ADU as the units have no impact on linearity.

Figure 4-18 shows the residual plot from device W1-1. The red lines represent the boundaries of 5% linearity, located at  $\pm 2.5\%$ . Linearity on the device is good, with the residual staying between  $\pm 1\%$  until  $\sim 2200$  ADU (73% FWC) and is linear to within 5% up to  $\sim 2750$  ADU (92% FWC).

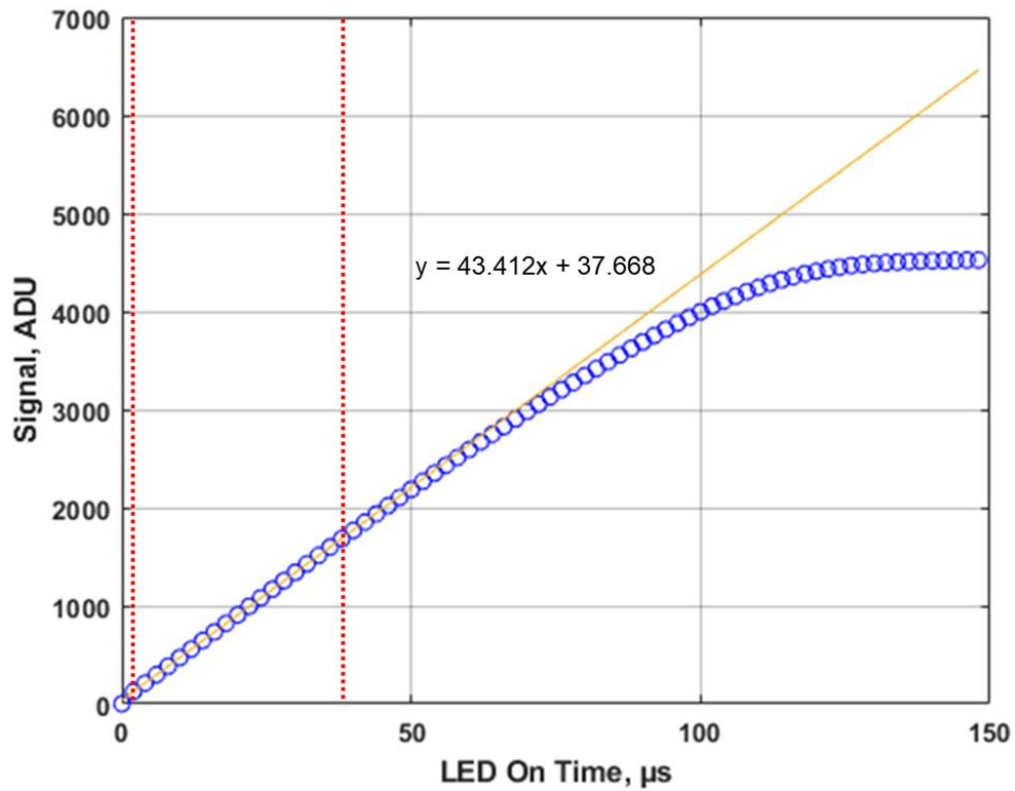


Figure 4-17: Signal against LED On Time for W1-1. The yellow line shows the trendline that is fitted to the straight portion of the graph, along with the equation. Red lines indicate the bounds of the data used to generate the line of best fit. Uncertainties are found to be too small to be visible on the figures and have negligible effect on linear fits.

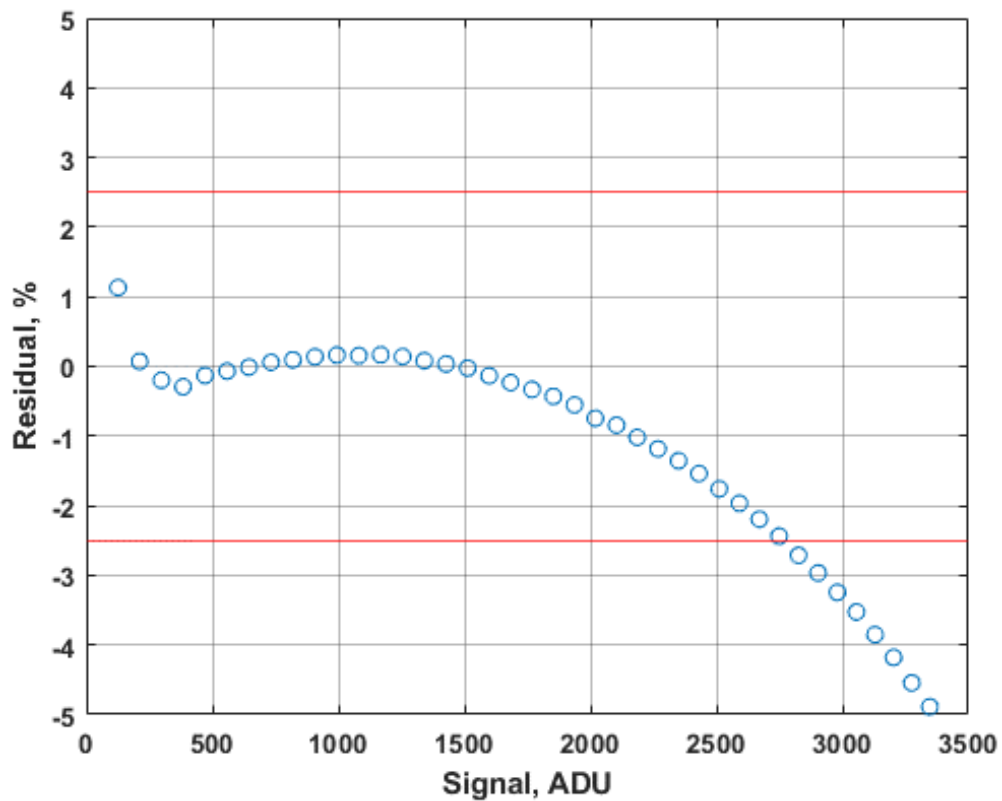


Figure 4-18: Residual plot for W1-1, demonstrating where it deviates from 95% linearity. The red lines are placed at  $\pm 2.5\%$  to show where the deviation occurs, in this case 2752 ADU or  $\sim 10,250 e^-$ .

The same measurements are done on the devices with the DDEs.

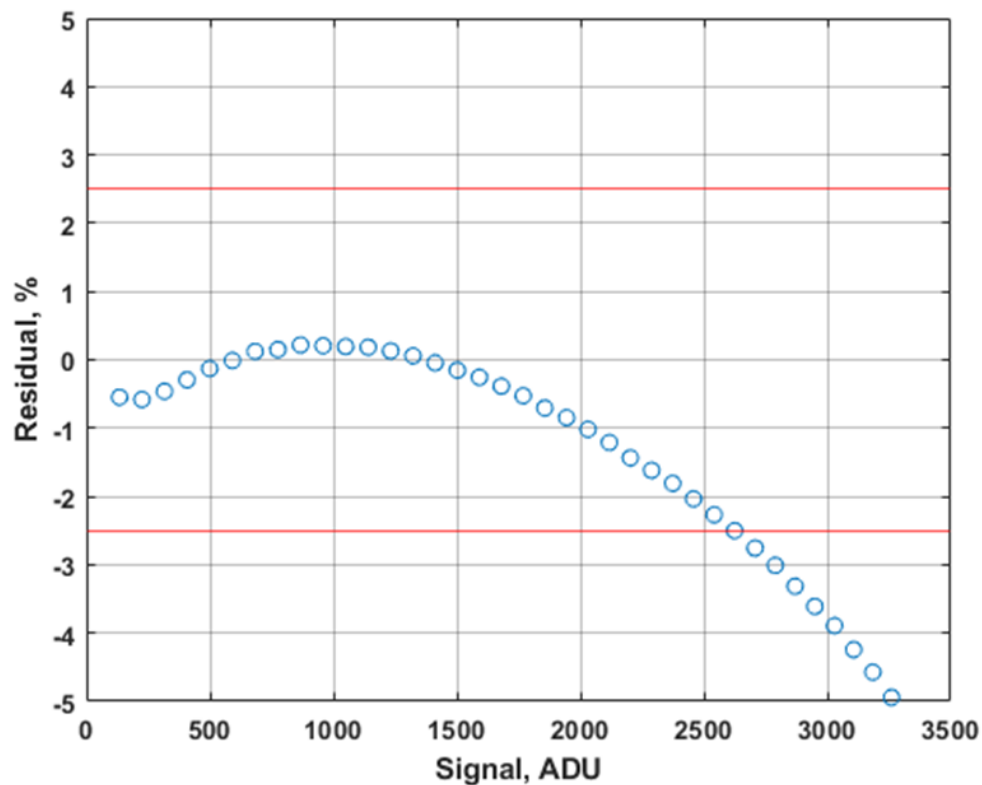


Figure 4-19: Residual plot for W3-1 with -4 V reverse bias.

W3-1 shows similar linearity characteristics to those of W1-1, shown in Figure 4-19. The deviation for  $\pm 1\%$  occurs at a slightly lower signal (2000 compared to 2200), as does the 5% linearity (2600 compared to 2750). These results are for the device under the maximum reverse bias. Results at 0 V are similar.

Figure 4-20 shows the residual plot from W11-1 with the maximum -8 V reverse bias. The plot shows almost identical linearity to that of W1-1, indicating that the modifications made to the pixel by introducing the DDE has negligible impact on the sensor's linearity.

Only a select few linearity measurements are shown here in the interest of brevity, but all of the sensors showed similar linearity characteristics to one another. The ones shown here are at the extremes of the implant range, so are the most likely to exhibit unusual behaviour.

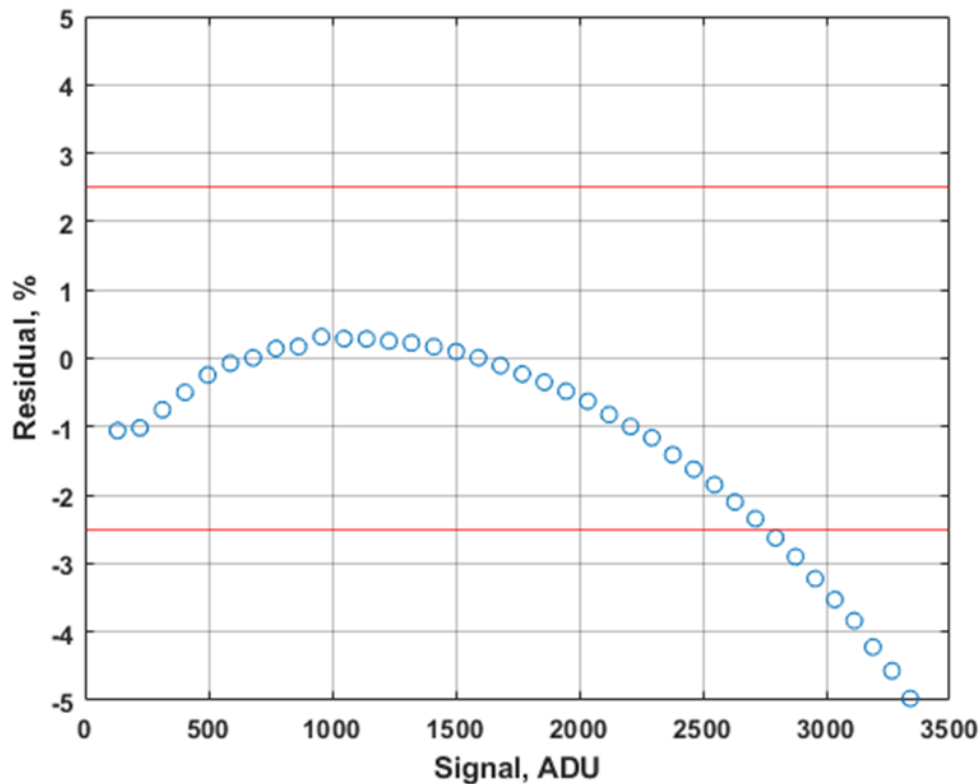


Figure 4-20: Residual plot for W11-1 with -8 V reverse bias.

The relationship between illumination and signal measured is not linear in any CMOS image sensor.

As can be seen in Figure 4-21, the relationship can be better approximated by a second order equation, with a very similar first order term to a linear fit. This equation has a residual of < 5% up to ~4250 ADU, or 95% of FWC, allowing for a much better prediction of the output signal for a given illumination level, although it does deviate more at low signal levels. The second order term accounts for the loss of linearity which occurs at high signals in solid state image sensors which can be attributed to the floating diffusion and the source follower.

The floating diffusion has a non-linear capacitance which varies with output voltage as  $1/\sqrt{V}$ . As the output voltage increases, the capacitance of the floating diffusion decreases, which in turn lowers the CVF. A lower CVF means fewer volts per electron, reducing the rate at which measured signal increases.

The source follower becomes non-linear at high signal levels due to the body effect and an induced lowering of the gain [1]. The body effect increases the threshold voltage of the source follower,

decreasing the voltage output of the pixel per electron in much the same way as the lowering CVF does.

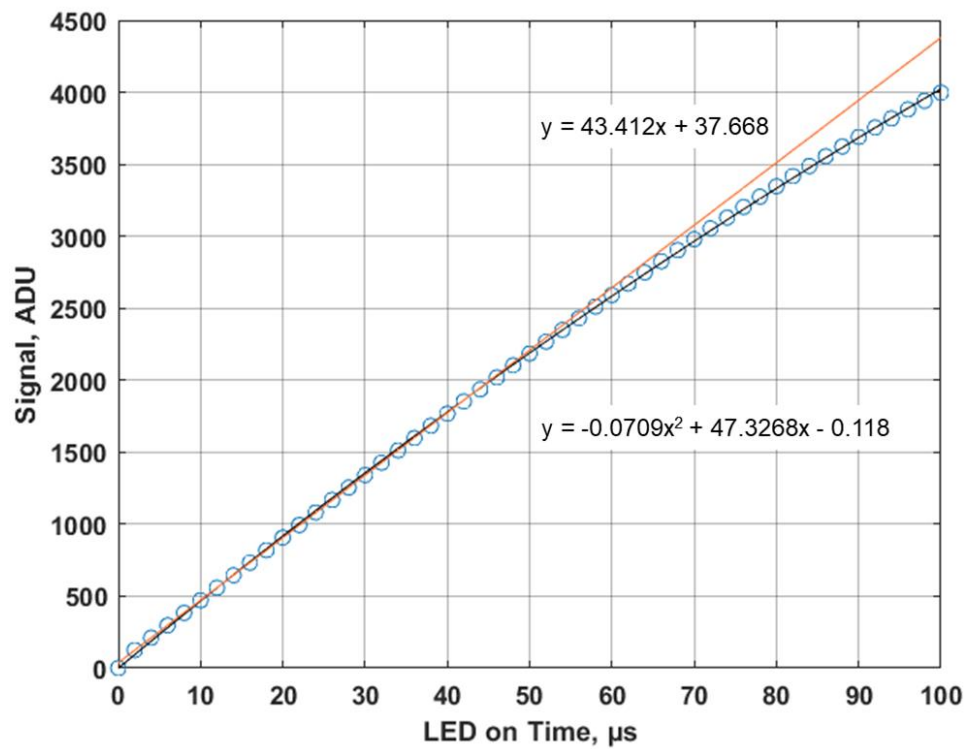


Figure 4-21: Signal curve of W1-1 with linear (orange) and second order (black) fits, which is up to 90% of the full well, before saturation begins. The equation above the curve is for the linear fit, whilst the equation below is for the second order fit.

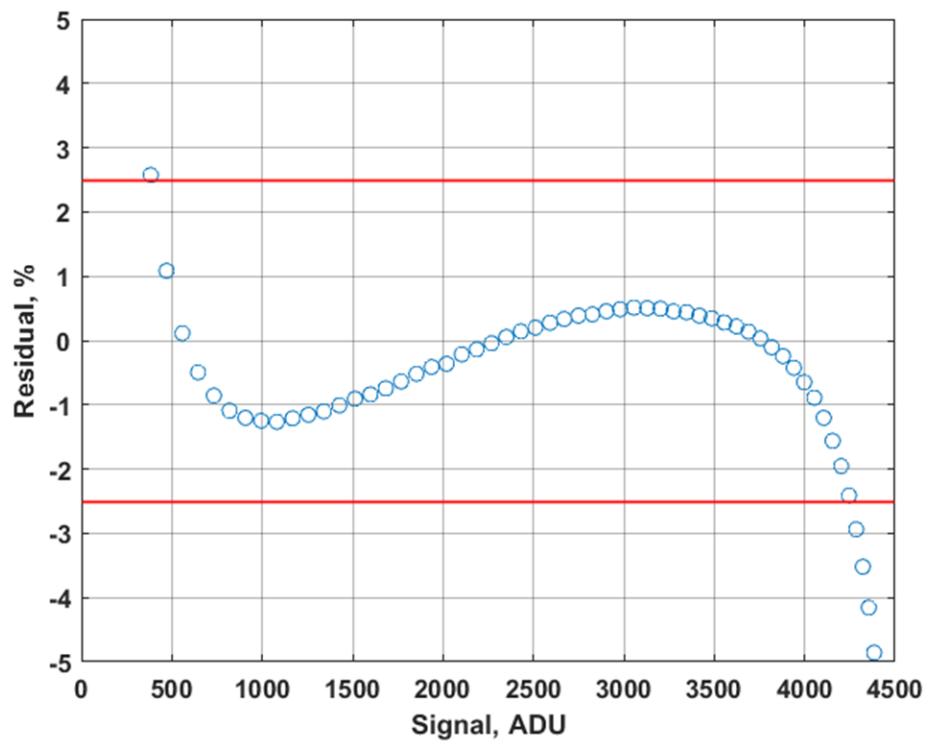


Figure 4-22: Residual plot for W1-1 using the second order curve.

## 4.6 Image Lag

As the DDE implants change the potential distribution in the pixel, it is important to verify their impact on the image lag. For the methodology of image lag measurements, please see Chapter 5. All tests are performed with a transfer gate voltage of 3.3 V, a reset voltage of 3.3 V and a transfer time of 2  $\mu$ s. For each device measured, the calculated gain is used to convert the signals into electrons for easier comparison.

Figure 4-23 shows the measured image lag in W1-1 in the first frame after image readout as blue circles. This will serve as the comparison for the rest of the sensors. Image lag is measured on all other devices at varying reverse biases, with results in the same figure for comparison.

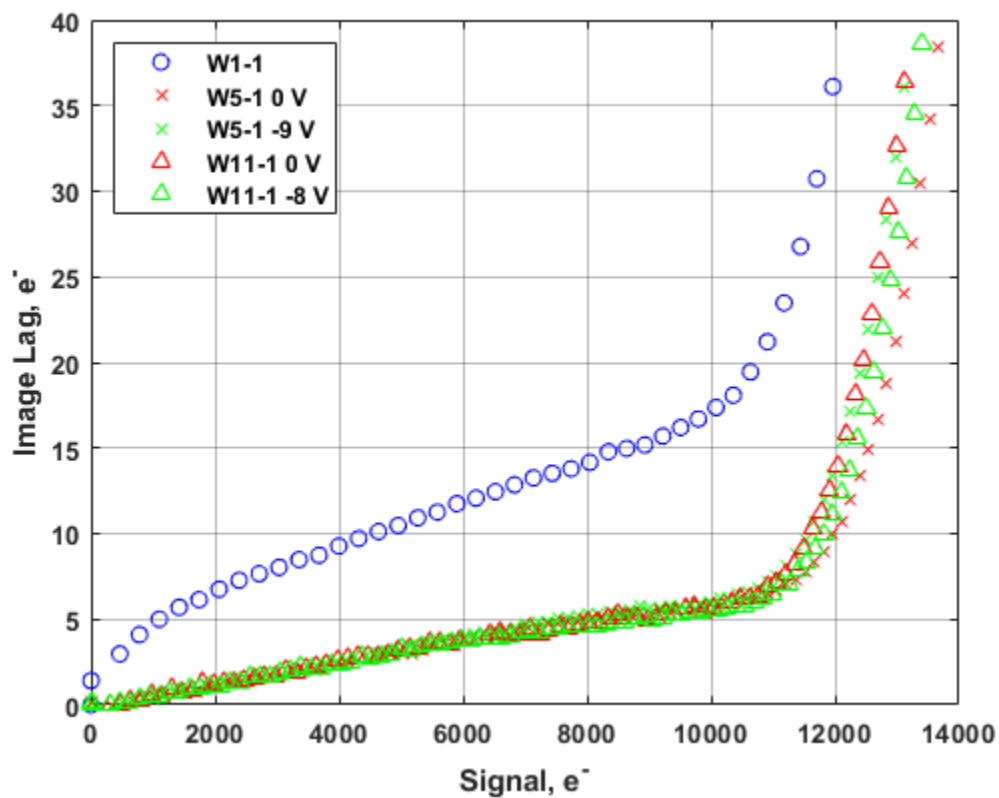


Figure 4-23: Image lag results from W1-1, W5-1 and W11-1 at varying reverse bias voltages.

The results indicate that image lag is lowered significantly with the addition of the DDE implant. The reasons for this improvement in image lag are unknown at this time. These results indicate that the additional potential caused by the DDE implant does not hinder charge transfer but instead



enhances it. The application of reverse bias also has a negligible effect on image lag, so any further lag tests can be done with full reverse bias.

## 4.7 Conclusions

Preliminary tests show that the BSB1 devices work as was predicted by the simulation work. The DDE implants are shown to suppress leakage current through the device, allowing significant reverse bias to be applied, thus extending the depletion region. The combination of high implant dose and high pinning voltage allows for the largest reverse bias to be applied. Variant W9 with high implant dose and high pinning voltage can be reverse biased up to -10 V with little leakage current, while W11 with the same implant but lower pinning voltage can be reverse biased up to -8 V. Variants W5 and W7, with medium implants and high and low pinning respectively, can be reverse biased up to -8 V and -6 V respectively. With the low implant and high pinning voltage, W3 can be reverse biased to -4 V and with no implant, W1 cannot be reverse biased without a large current flowing.

The PTCs generated for each device indicate that the optoelectrical characteristics of the modified devices are almost identical to that of a standard device fabricated to the same specifications. The full well capacities of the new devices are all equal to the standard device, at around  $11 \text{ ke}^-$ , as is the gain, between 3.705 and 3.897 for all devices. Linearity is unaffected by the new implant, with all variants maintaining 5% linearity to over 80% of full well capacity. Image lag appears to be largely improved by the additional implant, although the reasons for this are still unclear.

Due to the full depletion of the silicon, these new devices should reduce the amount of charge spreading between pixels, particularly at shorter wavelengths. It will also allow for much thicker, fully depleted CMOS sensors, greatly enhancing the quantum efficiency at longer wavelengths such as near-IR.

## 4.8 References

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## 5 Image Lag in CMOS Image Sensors

### 5.1 Introduction

Image lag is the incomplete transfer of photogenerated electrons from the photodiode to the floating diffusion during the readout process. The remaining electrons which are not transferred remain in the photodiode and are not measured in the current image. They are instead contained within the photodiode until the readout of the next image. The detriment to imaging from image lag is two-fold. First, any electrons which are not transferred in the readout of an image do not contribute to the signal being read, meaning a measured object may appear less bright than it actually is. Second, any electrons which remain in the photodiode after readout can contribute signal to the next image captured, resulting in a 'ghost' image, where features of the previous image are still visible in the subsequent image.

This chapter will focus on the measurement of image lag in the BSB1 CMOS devices. The effects of the transfer gate voltage and timing are investigated, as well as the floating diffusion reset voltage.

Results from a new method of reducing image lag by using more than one voltage applied to the transfer gate during readout are also presented here.

### 5.2 Sources of Image Lag

Image lag can arise from many different sources, from the physical attributes of the pixel to the voltages applied to the transfer gate and the sense node. This section details some of the main contributors to image lag and the theory behind them.

Thermionic emission theory states that the number of electrons left in the photodiode  $N_e$  after the transfer period is defined mathematically as [1]:

$$N_e = N_{e0} \exp \left[ -\frac{I_0}{qN_C V} \exp \left( -\frac{qV_{\Delta C}}{kT} \right) t \right] \quad (5-1)$$

Where  $N_{e0}$  is the number of electrons in the PPD before charge transfer,  $I_0$  is the initial emission current between the PPD and FD,  $q$  is the electron charge,  $N_C$  is the conduction band effective density of states,  $V$  is the volume of the PPD,  $V_{\Delta C}$  is the barrier height on the charge transfer path,  $k$  is the Boltzmann constant,  $T$  is the absolute temperature and  $t$  is the charge transfer time. This equation will be used in the following sections to quantify the lag from various sources.

### 5.2.1 Size of the Photodiode

To maximise the number of photons captured during the integration period, the size of the photodiode, and therefore pixel, should be as large as possible. This can improve the low light capabilities, increase the full well capacity and signal to noise ratio of the sensor. These benefits are gained at the loss of spatial resolution in the images produced. An increase in the area of a photodiode can also lead to an increase in image lag [2]. As the photodiode gets larger, the distance between the transfer gate and the furthest point in the photodiode increases. When a voltage is applied to the transfer gate, it creates an electric field that draws the electrons from the photodiode to the floating diffusion. The lateral field strength decreases with distance and so the further the electrons are from the transfer gate, the less pull they will feel. This limits the transfer of electrons to diffusion [3], a slow process which can lead to incomplete charge transfer unless long transfer times are used. This can be seen mathematically in Equation (5-1) in the factor  $V$ , the volume of the photodiode. As the volume increases, the number of electrons that remain in the photodiode after transfer increases.

### 5.2.2 Transfer Gate Voltage

The purpose of the transfer gate is to contain the electrons during charge integration by means of a potential barrier, then transfer the charges to the floating diffusion where they can be read out. This transfer is achieved by applying a voltage to the transfer gate in order to lower the potential barrier and create an electric potential beneath the transfer gate. This potential serves to actively draw the electrons from the photodiode into the floating diffusion, speeding up the transfer process. A diagram of the potentials during charge integration and transfer is shown in Figure 5-1.

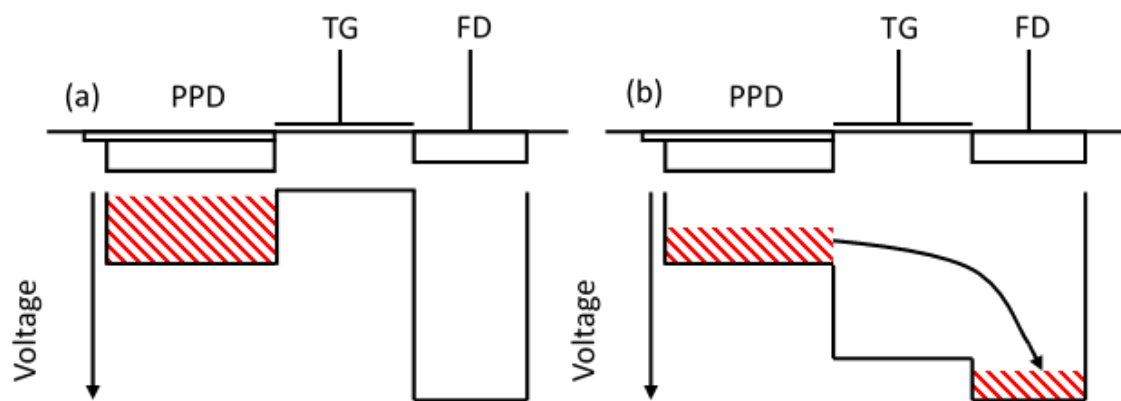


Figure 5-1: Potentials of the photodiode, transfer gate and floating diffusion a) during charge integration and b) during charge transfer.

Since the strength of the potential under the transfer gate is directly proportional to the voltage applied to the transfer gate, a more positive voltage leads to a faster transfer of electrons [4]. This can be inferred from Equation (5-1), where an increase in  $I_0$  leads to a decrease in the number of electrons which are not transferred. Subthreshold MOSFET theory states that as the voltage between gate and source increases, so does the current between the drain and source [5]. Therefore, as the transfer gate voltage increases, so does the emission current. The transfer gate voltage cannot be arbitrarily increased however, as will be discussed later.

### 5.2.3 Transfer Gate 'on' Time

The transfer of electrons from the photodiode to the floating diffusion is not instantaneous. The transfer gate needs to be 'on' - have a voltage applied to it - for a finite amount of time in order to fully transfer the charges.

The influence on the number of charges transferred that the “on time” has is shown in Equation (5-1), as the variable  $t$ . The relationship is exponential in nature, meaning that the majority of electrons are transferred early on in the process, whilst the remaining charges slowly trickle across. This arises from the physical location of the charges within the photodiode. Any charges close to the transfer gate will be drawn across by the induced electric field when it is turned on, whilst charges further away are limited to thermal diffusion until they are sufficiently captured by the electric field, at which point they will be transferred [6].

The length of time that the transfer gate is on must be carefully considered when choosing the operating parameters. For high frame rates, the transfer time needs to be kept to a minimum, but if the transfer time is too short, the number of residual electrons in the photodiode will be high. The exponential nature of the rate of charge transfer, shown in [6] and mathematically in Equation (5-1), means that as transfer time is increased, the associated charge transfer increase is negligible. The transfer gate on-time should be carefully considered to minimise lag but not affect the frame rate.

#### 5.2.4 Potential Barriers and Pockets

In an ideal pixel, the path an electron takes during charge transfer is a smooth transition from an area of low electrostatic potential to one of higher potential. In a real pixel however, there may be small areas where the potential is uneven and can hinder the movement of electrons. These may be introduced during the design and manufacturing stage or caused by radiation damage.

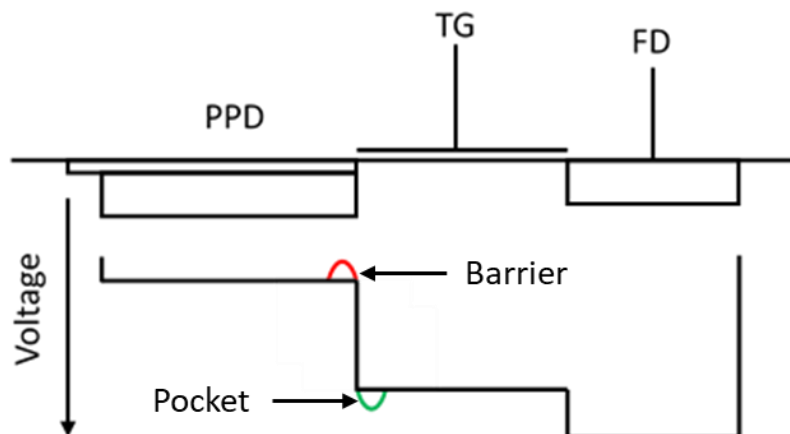


Figure 5-2: A simplified representation of the electrostatic potential in a CMOS pixel containing potential barriers and pockets. The ideal potential is shown in black, with a potential barrier on the edge of the PPD shown in red and a potential pocket under the TG shown in green.

Potential barriers, shown in red in Figure 5-2, can increase the measured image lag by stopping electrons passing over them. A potential barrier is an area of lower electrostatic potential. Electrons build up on one side of the barrier, with only a small number emitted thermally, which is a slow process, the rate  $J$  of which is given by:

$$J = A^* T^2 e^{\left(-\frac{q\Phi_B}{kT}\right)} e^{\left(\frac{qV}{kT}\right)} \quad 5-2$$

Where  $A^*$  is the effective Richardson constant for thermionic emission neglecting the effects of optical phonon scattering and quantum mechanical reflection,  $\Phi_B$  is the barrier height and  $V$  is the applied external voltage reducing the barrier height.

When enough electrons are generated, they will spill over the barrier. The number of electrons held by the potential barrier is determined by its height. If the electrons build up on the photodiode side of the barrier, these electrons are measured as image lag.

Potential pockets work in a similar fashion but are areas of increased electrostatic potential. Electrons trapped in the pocket of higher potential, as with the barrier, may slowly thermally emit from the pocket. When enough charge is trapped such that the overall potential is lower, any additional electrons will pass over it. When the transfer gate is switched off, the electrons trapped in the pocket will diffuse away. If these electrons move back into the photodiode, they will be measured in the next image as lag.

Lag from these barriers and pockets will not be discussed further in this chapter, but more information can be found in [7]-[11].

### 5.2.5 Charge Spillback

As charge is transferred from the photodiode to the floating diffusion, the potentials within the pixel are under constant change. After reset, the floating diffusion is at its greatest potential. After charge integration, the photodiode is at its minimum potential (assuming full well has been reached). This is shown in Figure 5-3 (a). When a voltage is applied to the transfer gate, the potential barrier is

lowered, and the potential gradient induced will attract electrons from the low potential of the photodiode to the high potential of the floating diffusion, as shown in Figure 5-3 (b).

As the electrons move into the floating diffusion, its electrostatic potential is decreased. The potential is decreased further as more electrons are added until the point where the potential in the floating diffusion and under the transfer gate are roughly equal. At this point the electrons will have no preference as to which area the charge cloud will collect and will spread out underneath the transfer gate, shown in Figure 5-3 (c).

Once the transfer period has finished and the transfer gate is returned to ground, the electrons that were spread underneath it will be drawn to the nearest area of high potential. If the electrons had spread far across the transfer gate, to the side closest to the photodiode, they have a chance of being drawn back into the photodiode, resulting in spillback and image lag. This is shown in Figure 5-3 (d).

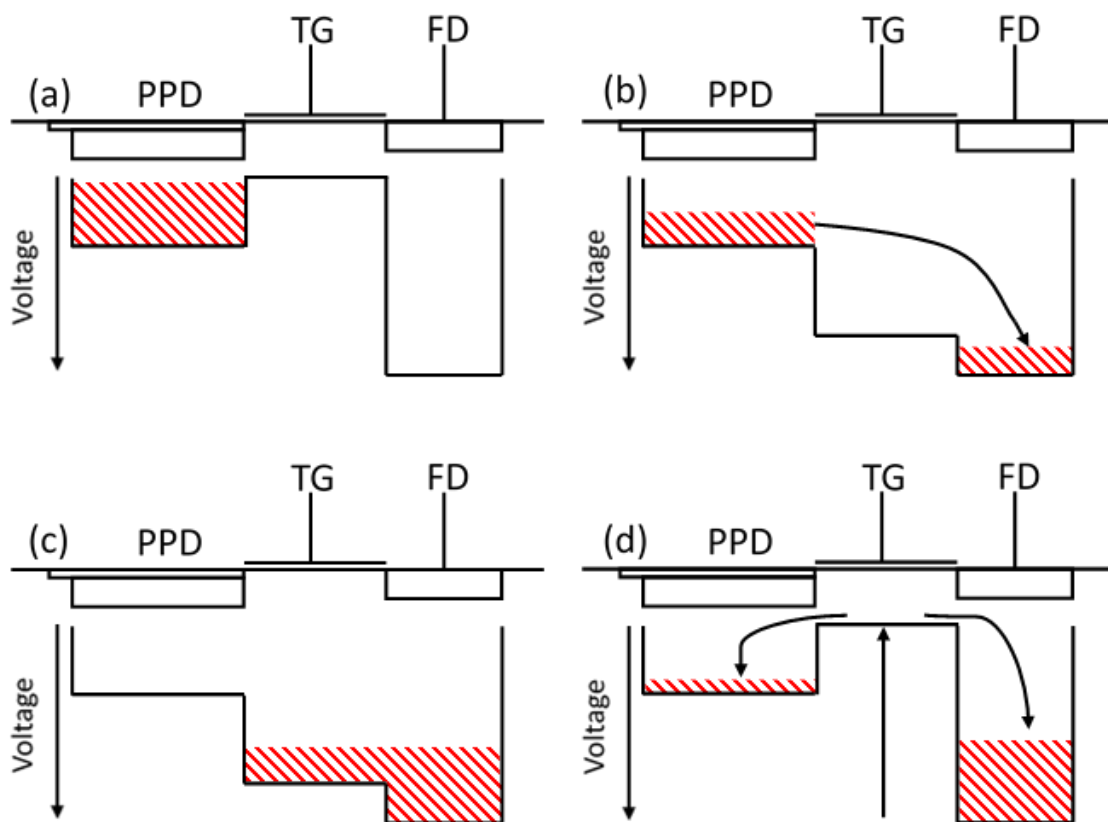


Figure 5-3: Diagram of pixel potential and charge movement during, a) charge integration b) charge transfer c) charge spreading and d) charge spillback. Red hatched markings represent the charge cloud.



Charge spillback can also influence linearity measurements [12] and affect photon transfer curves.

As the average signal reaches the level where spillback first occurs, the pixels affected will remain at the same signal level even as illumination levels increase. The pixels that did not have enough signal to begin spillback will continue gaining signal until they too begin spillback. This causes a reduction in variance between the pixels until the illumination level is high enough that spillback has been reached in all pixels and variance increases again. This is illustrated in Figure 5-4.

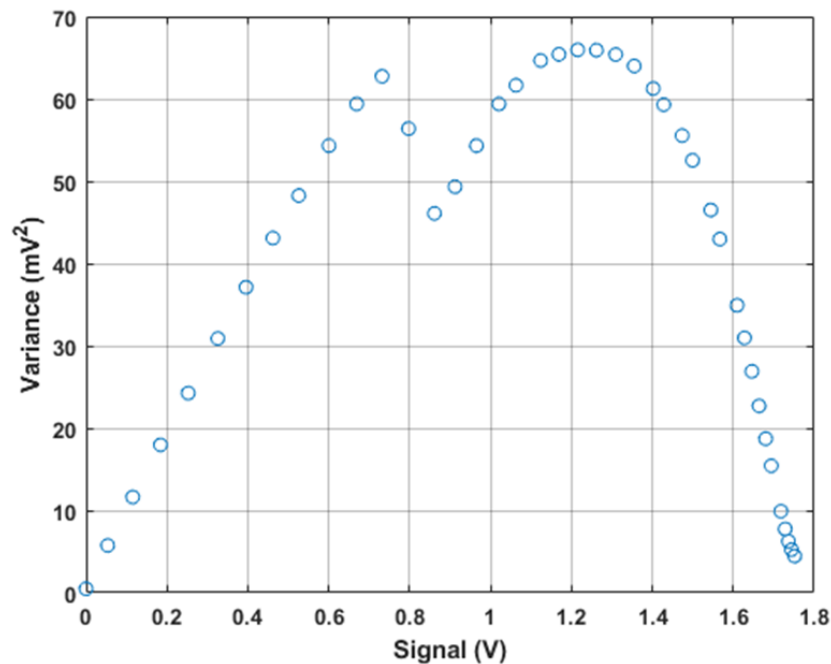


Figure 5-4: An example of a decrease in variance caused by charge spillback in CIS113. Data taken from earlier work by the author.

### 5.3 Current Methods of Lag Reduction

Current efforts to reduce image lag in CMOS sensors currently focus on two main areas – pixel design and operating parameters.

When large pixels are needed for low light or high-speed situations, the large photodiode can lead to increased image lag as discussed earlier. To combat this, novel pixel designs have been introduced to counteract the associated increase. In [2], [3] and [13] new photodiode shapes are developed which help by moving electrons from the far side of the photodiode to the transfer gate. This is achieved by changing the shape and introducing a weak electric field within the photodiode, causing electrons further away to still be drawn to the transfer gate. Some examples of the novel photodiode shapes

used in [13] are shown in Figure 5-5. The finger shaped PPDs found in (c), (d) and (e) increase the electric field in the direction of the TG, reducing image lag.

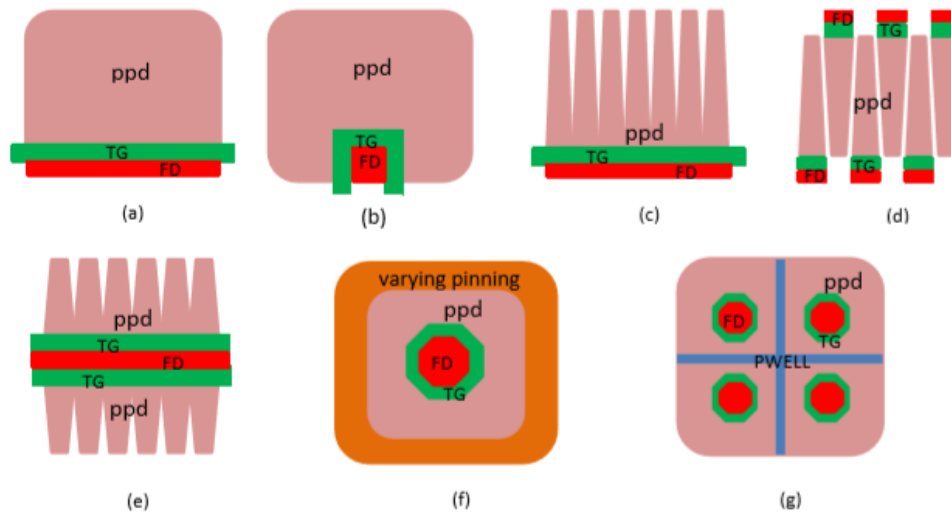


Figure 5-5: Examples of novel photodiode and transfer gate shapes designed to decrease image lag in large photodiodes [13].

Other pixel designs focus on the transfer gate for reducing lag. In Figure 5-5 there are a number of different transfer gate shapes, sizes and locations within the pixel. These include a transfer gate in the centre of the pixel, as well as U-shaped transfer gates (as opposed to the standard rectangular shape). The purpose of these designs is twofold – to increase the field strength in the direction of charge transfer and to minimise diffusion distance inside the photodiode. For example, pixel (f) in the figure reduces image lag by effectively halving the maximum distance that the electrons must travel in the photodiode before reaching the transfer gate.

Another transfer gate design which can be employed to reduce image lag is to alter the doping under the transfer gate. In [14] an added N-doped region in the photodiode and two separate P-doped regions under the transfer gate are used to create a stepped profile in the direction of the floating diffusion, shown in Figure 5-6. This serves to decrease spillback induced lag by keeping the spillback electrons on the floating diffusion side of the transfer gate so that when it is turned off, they are more likely to go into the floating diffusion and be read out. [15] and [16] use a similar technique but it is more of a smooth decrease in potential from the photodiode to the floating diffusion and serves the same purpose.

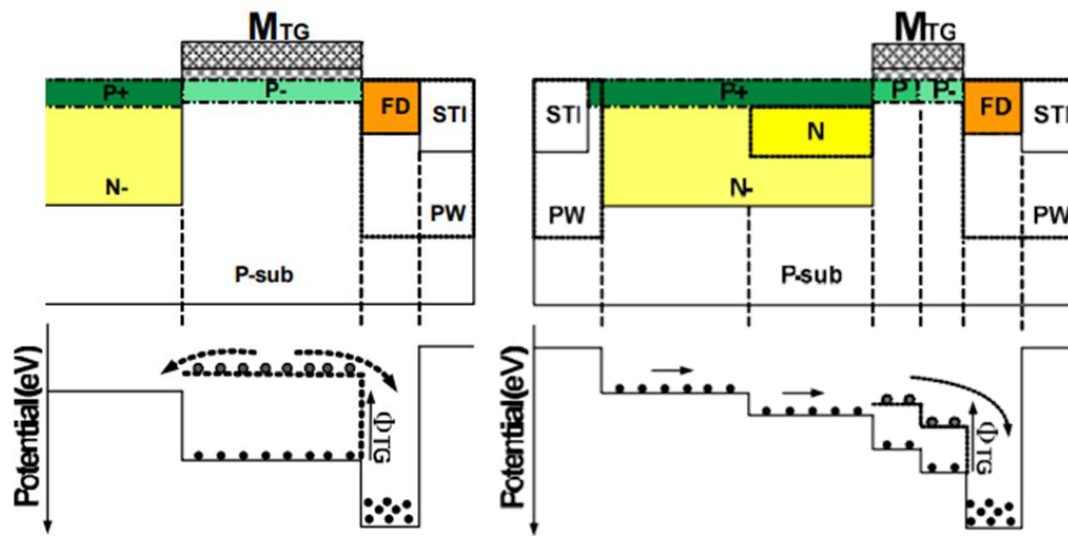


Figure 5-6: Pixel layout and potential diagram showing lag reduction technique used in [14]. The left-hand pixel is a standard CMOS pixel, whereas the right-hand pixel shows the stepped potential used to minimise image lag.

Other work focusses on modifying timings and voltages in existing devices to reduce the image lag.

This has the advantage of being cheaper and faster, and can be done on off the shelf components, as well as in optimising image sensors for use in space missions. [17] discusses a simulation in which the transfer gate voltage is modified in order to minimise the effects of image lag. Different timing sequences, such as pulsing the transfer gate before reset, may also be used on the transfer gate in order to reduce the effects of image lag as in [6].

## 5.4 Experimental Details

This section details the experimental procedures and apparatus used for data collection regarding image lag.

### 5.4.1 Experimental Setup

To measure image lag, the sensor is uniformly illuminated across all pixels by an LED. This is achieved via an LED, controlled through software, shining through a ground glass diffuser. The diffuser spreads the light more evenly than having the LED shine directly onto the sensor, ensuring a more uniform pixel illumination.

### 5.4.2 Lag Frame Capture

To measure image lag at different illumination levels, first a series of bright images were taken with increasing LED on time after each cycle. Within each cycle, 100 images are taken and the mean pixel value for all the images calculated.

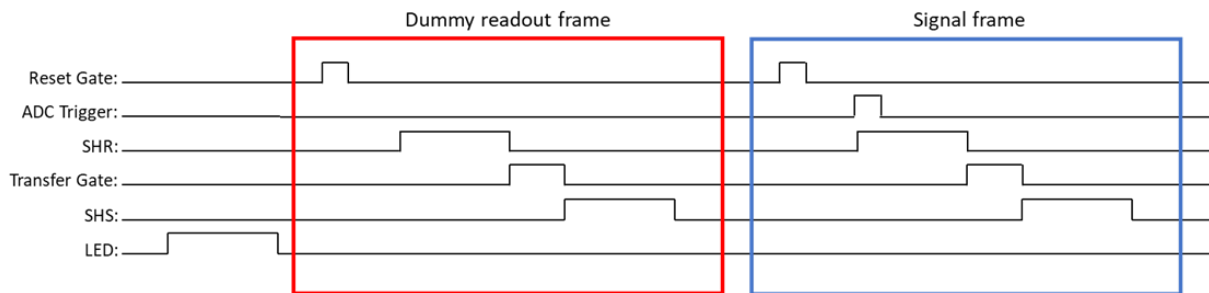


Figure 5-7: Timing diagram for image lag measurement. Dummy readout is shown after the LED pulse, inside the red box. There is no ADC trigger, so no data is recorded for this frame. In the blue box is the signal frame, where the ADCs are triggered, and data is recorded.

To generate the lag data, the parameters are all kept constant and a dummy readout is added after the LED illumination period. This is done by doing a full readout of the sensor without activating the ADC circuitry, thus no data is recorded. A normal readout with the ADCs activated is performed after the dummy readout, recording data and measuring the image lag, shown in Figure 5-7.

## 5.5 Image Lag Measurements

This section describes tests performed to measure the effect of the transfer gate on lag, both in the voltage applied and the time the voltage is kept high for. All tests in the section are carried out with a single transfer gate “on voltage” per transfer.

### 5.5.1 Transfer Gate High Voltage Dependence

To test the effect of the transfer gate high voltage ( $VTG_H$ ) on lag, all other parameters are kept constant. These include a transfer gate on time of 15  $\mu s$ , transfer gate low voltage ( $VTG_L$ ) of 0 V, a reset voltage of 3.3 V and the same timing sequence. Since it was discovered that the reverse bias had no effect on the lag, the reverse bias was kept at its maximum value of -6 V.

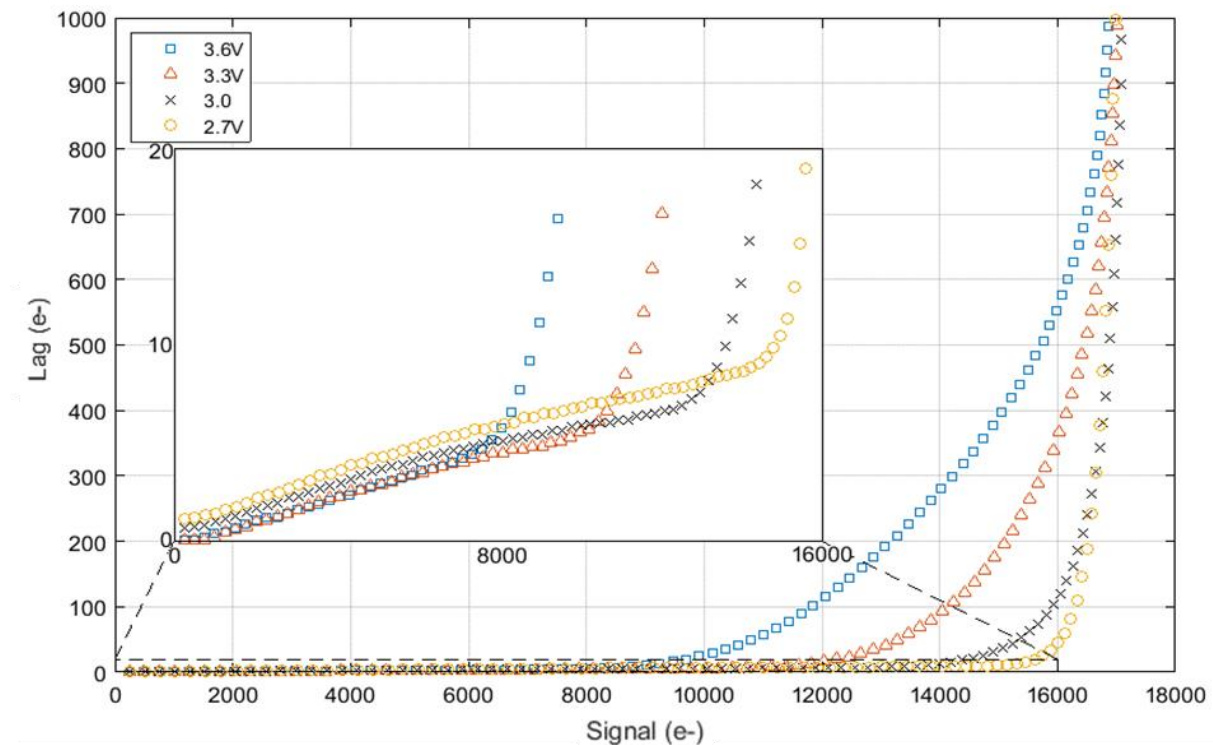


Figure 5-8: Lag measurements with varying  $VTG_H$ . The inset graph shows a zoomed in portion of the larger graph.

Results for the  $VTG_H$  tests are shown in Figure 5-8. For low signal levels, the results show that as the transfer gate voltage is increased, the lag decreases. This agrees with the theory, as a higher voltage induces a stronger field which draws more electrons across. At  $VTG_H < 2.7$  V the potential under the transfer gate is not high enough and results in lag much higher than the values shown in the figure.

At signal levels  $> 10,000$   $e^-$ , the image lag signal increases dramatically due to charge spillback. The point at which this occurs is directly linked to  $VTG_H$  and occurs at higher signals for lower gate voltages. This supports the theory shown in Figure 5-3, as the difference in potential between the floating diffusion and under the transfer gate is larger, so more electrons can gather in the floating diffusion before spreading out under the transfer gate.

The result of this is that higher transfer gate voltages give lower image lag values at low signal levels, but a low transfer gate voltage gives low lag values at higher signal levels. This means that the transfer gate voltage could be adjusted depending on the expected signal levels.

### 5.5.2 Transfer Time Dependence

For testing the dependence of image lag on the time the transfer gate is held high,  $t_{TGH}$ , only this parameter is changed throughout the tests. With the previous section indicating that  $VT_{GH} = 2.7$  V gave the lowest lag to high signal levels, this was chosen to be the voltage used throughout. The reset voltage was kept at 3.3 V,  $VT_{GL} = 0$  V and reverse bias was -6 V.

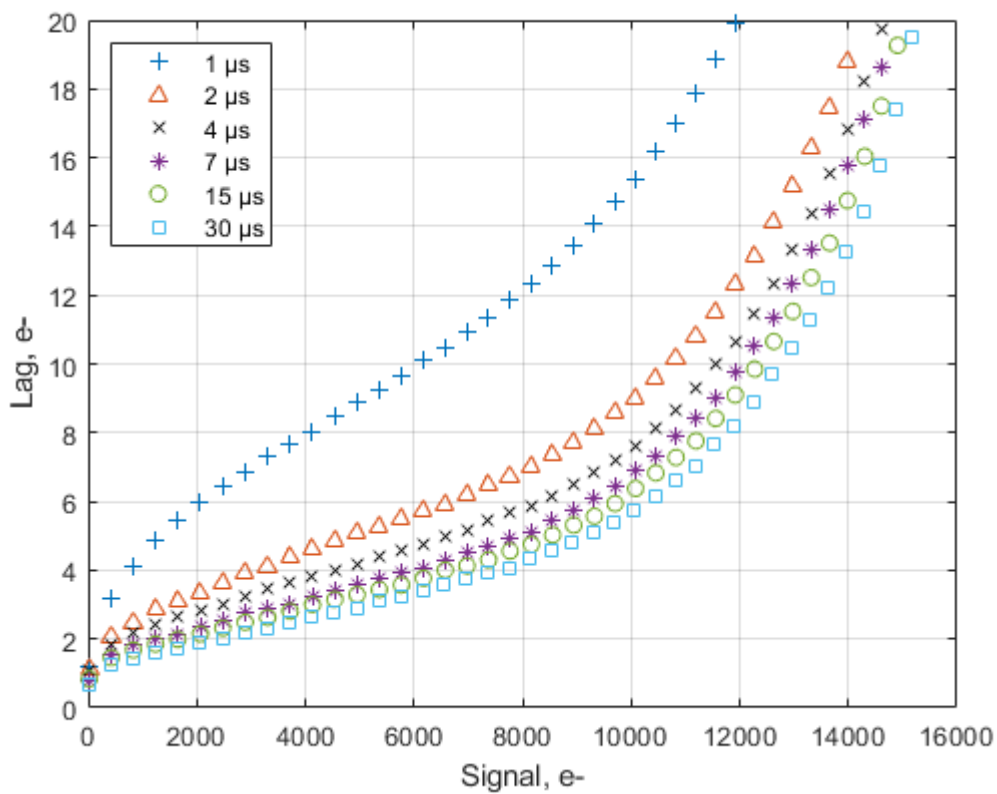


Figure 5-9: Image lag measured with varying transfer gate on times. Increasing the time on offers diminishing returns in image lag. All results taken at  $VT_{GH} = 2.7$  V, reset voltage = 3.3 V.

Figure 5-9 shows the results for image lag measured with varying  $t_{TGH}$ . The image lag improves as the time is increased in every case, and the amount it improves gradually diminishes as the time is increased further. These are the expected results, as the number of electrons left in the photodiode after transfer is logarithmically proportional to the time that the transfer gate is turned on for.

Image lag results were taken from select signal values and compared in Figure 5-10. Apart from the  $1\ \mu\text{s}$  values, the results follow a straight line when plotted with the time on a log scale. This appears to match well with the theory in Equation (5-1).

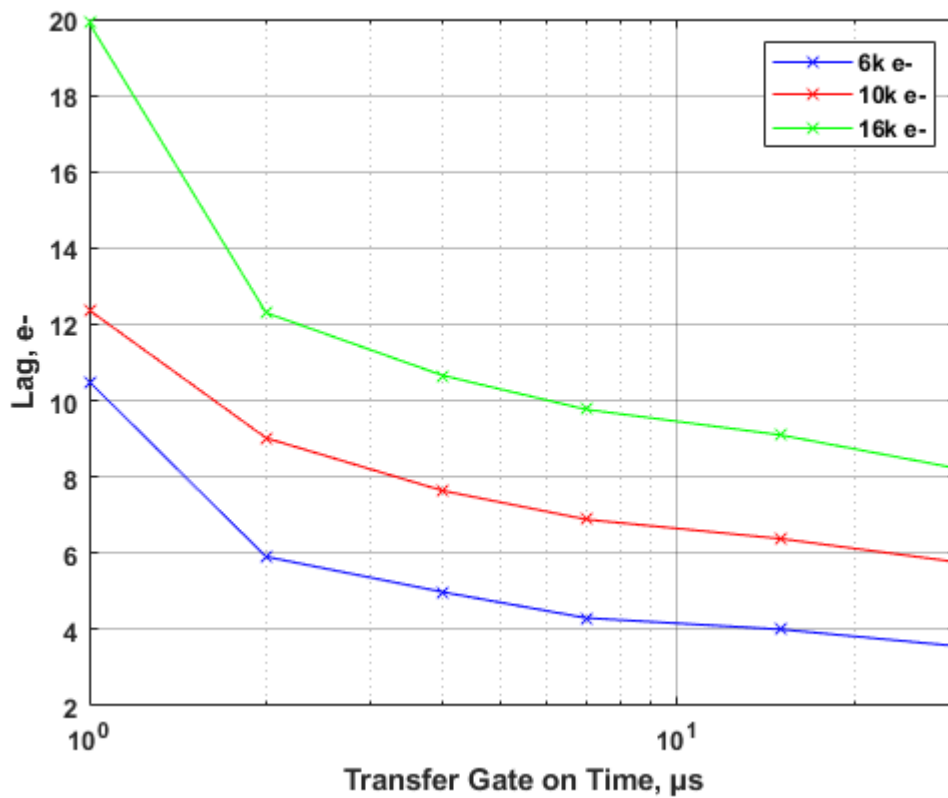


Figure 5-10: Image lag values against transfer gate on time taken at arbitrary signal values. Apart from  $1\ \mu\text{s}$ , all image lag values follow a logarithmic decrease with increasing transfer gate on time.

## 5.6 Reset Level – Voltage Measurements

To further test the theory of charge spillback, lag measurements were taken at different reset levels on the floating diffusion. Since spillback occurs when the potential in the floating diffusion reaches similar levels to that under the transfer gate, altering the initial potential should have an impact.

Results are shown in Figure 5-11.

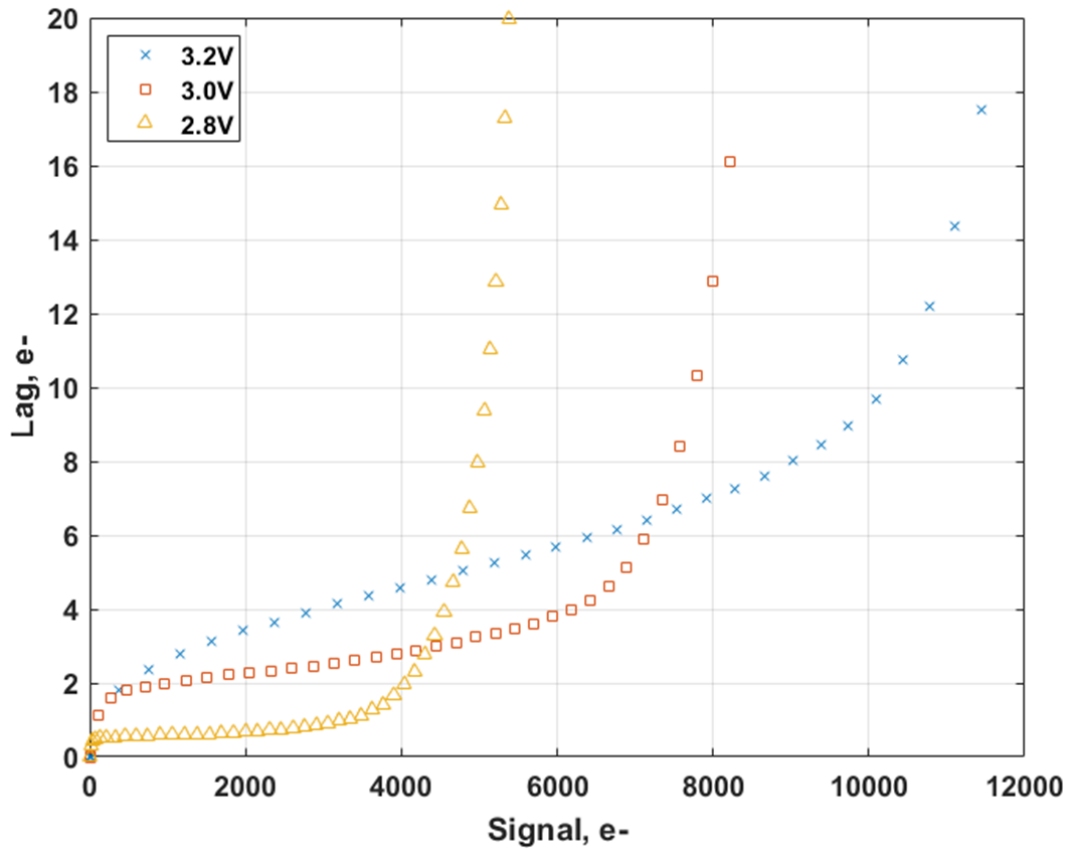


Figure 5-11: Measured image lag at different floating diffusion reset voltages. All tests run at  $VTG_H = 3.3$  V.

These results show that a lower reset level on the floating diffusion does reduce the signal level at which charge spillback occurs. This is due to the reduced number of charges required in order to bring the potential of the floating diffusion up to the point at which spillback will occur.

Using the conversion gain calculated in Chapter 4,  $79.3 \mu\text{V}/e^-$ , the difference in the signal at which spillback dominates can be matched up to the different reset voltages. The onset of spillback is  $\sim 3.9 \text{ ke}^-$ ,  $6.5 \text{ ke}^-$  and  $9.1 \text{ ke}^-$  for 2.8 V, 3.0 V and 3.2 V respectively. The difference between these is  $\sim 2.6 \text{ ke}^-$ , which when multiplied by the conversion gain gives 0.205 V, matching the difference between the reset levels.

## 5.7 Device Simulation

Simulations of the device were done in Silvaco Atlas Software [18] in order to probe the movement of electrons during the charge transfer process. Multiple transfer gate voltages were used, including single level and two-level.



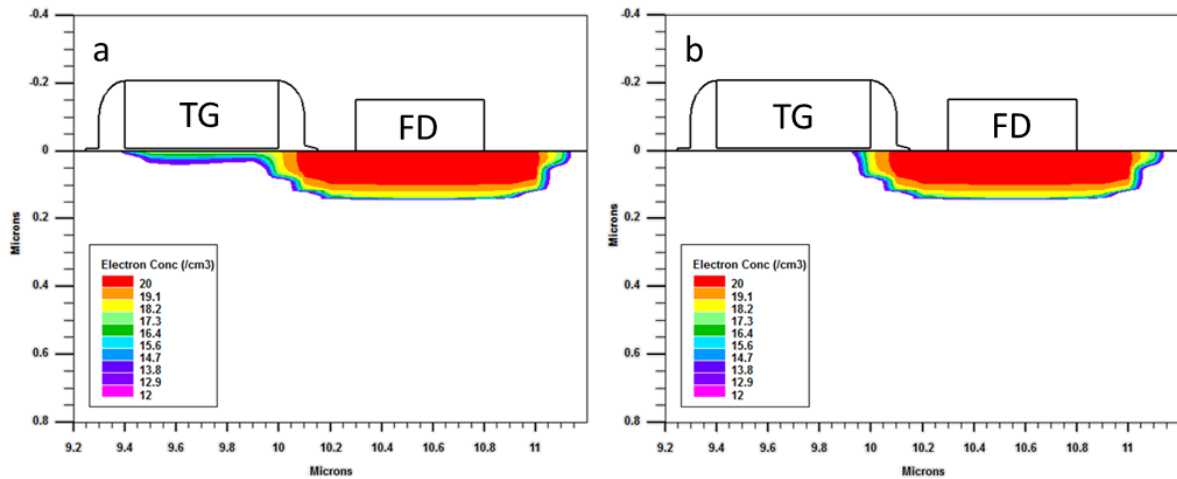


Figure 5-12: Simulated electron density during the charge transfer process in the floating diffusion and under the transfer gate: (a) at  $VT_{GH} = 3.6$  V, (b) at  $VT_{GH} = 2.7$  V. Charge can be seen spreading out from the floating diffusion and under the transfer gate at the higher voltage. The legend shows the logarithm of the electron concentration.

Figure 5-12 shows the density of electrons at the end of the transfer process in simulations for two  $VT_{GH}$  levels. The figure shows the density of electrons at the end of the transfer process, while the transfer gate is still high. At  $VT_{GH} = 2.7$  V (Figure 5-12 (b)), the electron cloud is almost completely in the floating diffusion, with none under the photodiode side (left-hand side) of the transfer gate.

When the transfer gate is turned off, the electrons will remain in the floating diffusion.

In Figure 5-12 (a) when the transfer gate is biased higher, the electrons have spread into the area of higher potential under the transfer gate itself, through to the side closest to the photodiode. Once the transfer gate is turned off and the potential returns to zero, the electrons on the photodiode side of the transfer gate are likely to spill back into the photodiode, resulting in image lag.

Further simulations showed that lowering the reset voltage applied to the floating diffusion before charge transfer gives similar results to having a high  $VT_{GH}$  – a higher concentration of electrons on the photodiode side of the transfer gate. This further supports the theory that the cause of the spread of electrons is due to a decrease of electrical potential in the floating diffusion due to increased charge transferred to it.

## 5.8 Multi-Level Transfer Gate

As seen in the transfer gate voltage dependence results, both high and low  $VTG_H$  have inherent advantages associated with them. A higher voltage applied to the transfer gate achieves lower values of image lag when signal levels are low. They do however become spillback dominated at lower signal levels than a lower voltage does. This leads to different voltages being useful in different situations. The purpose of a two-level transfer gate voltage is to combine the advantages of both regimes with none of the drawbacks.

### 5.8.1 Two-Level $VTG_H$

To deliver multiple  $VTG_H$  levels in a single readout pulse, some modifications had to be made to the readout circuitry. In a standard readout mode, a single voltage is constantly supplied to the chip. The voltage is applied to the transfer gate through a switch on-chip which is controlled via software. To apply two voltages in a single readout, a switch was added off-chip, also controlled by software, with the two voltages as inputs and the output leading to the transfer gate. This switch is shown in Figure 5-13 as SW1. The capacitance of the circuit was kept to a minimum to allow for fast switching between the two voltages.

The two-level  $VTG_H$  decreases lag by using a high voltage at the beginning of the transfer to draw the majority of electrons into the floating diffusion quickly. The voltage is then lowered to  $VTG_M$ , which increases the potential difference between the transfer gate and the floating diffusion. Any electrons which had spread under the gate will then be drawn to the floating diffusion, decreasing the effect of charge spillback.

An example of the resulting voltage applied to the transfer gate during readout is shown in Figure 5-14, represented by a solid black line.

### 5.8.2 Ramped Down $VTG_H$

To further the idea of a multi-level transfer gate, a ramped down transfer gate voltage was employed. Instead of using two discrete voltages with a fast switch between the two, a continuous voltage ramp is introduced in the transition between  $VTG_H$  and  $VTG_M$ .

To achieve this ramped voltage decay, further modifications were made to the board. An RC circuit was added between SW1 and the chip, as shown in Figure 5-13. The variable resistor (0 – 11 k $\Omega$ ) enables control over the decay rate of the voltage, allowing different transfer gate timings to be used. Two examples of the voltage applied to the transfer gate during readout are shown in Figure 5-14, the solid line representing a low resistance on the variable resistor and the dashed line a higher resistance.

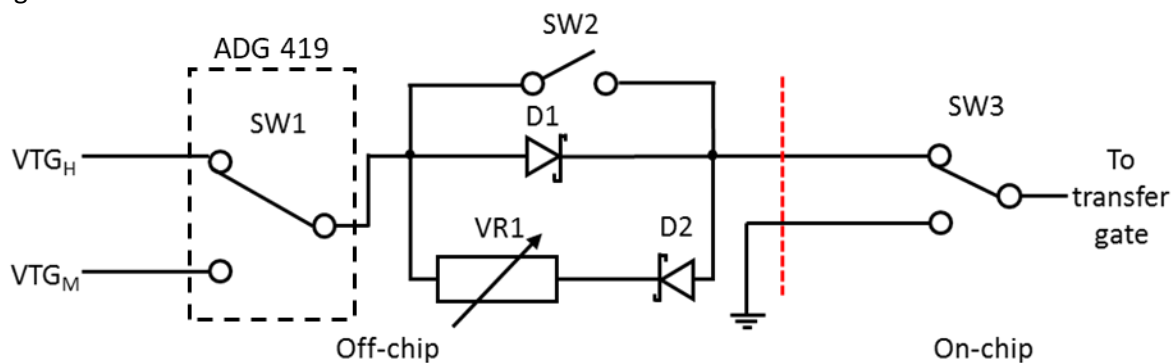


Figure 5-13: Circuit diagram of modifications made to the camera board in order to achieve both the two-level and decaying  $VTG_H$ . Switch 1 allows the transition between the two  $VTG$  levels. Diodes 1 and 2 combined with the 11 k $\Omega$  variable resistor facilitate the voltage decay method. Switch 2 allows for the voltage decay circuitry to be bypassed. Switches 1 and 3 are both controlled by software.

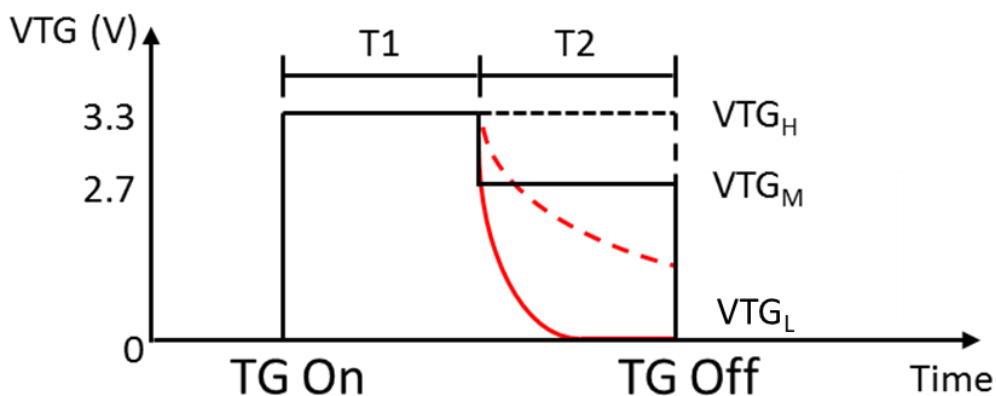


Figure 5-14: Simplified representation of the voltages applied to the transfer gate during readout. All readout schemes are the same during T1. The dashed black line shows a single level transfer gate readout. The solid black line in T2 shows the voltages in a two-level readout. The red lines show a ramped down voltage, the solid line with a low resistance and the dashed line for a higher resistance.

## 5.9 Two-Level Transfer Gate Voltage Measurements

Since the majority of charge is moved from the photodiode to the floating diffusion early in the transfer period, the starting voltage on the transfer gate should be high to maximise the rate of charge transfer. This initial high voltage is referred to as  $VTG_H$ . Once the bulk of charges have been transferred, the voltage is changed to an intermediate value between the off value, generally 0 V, and  $VTG_H$ . This middle voltage is labelled  $VTG_M$ . The transfer gate is then kept at  $VTG_M$  for the rest of the transfer period, until it is returned to the off state.

An advantage that this method of image lag reduction has is that it can be applied to virtually any existing CMOS sensor with only minor modifications to the external electronics. This makes it a quick and cheap method for increasing charge transfer efficiency.

### 5.9.1 Voltage Dependence – Two-Level $VTG_H$

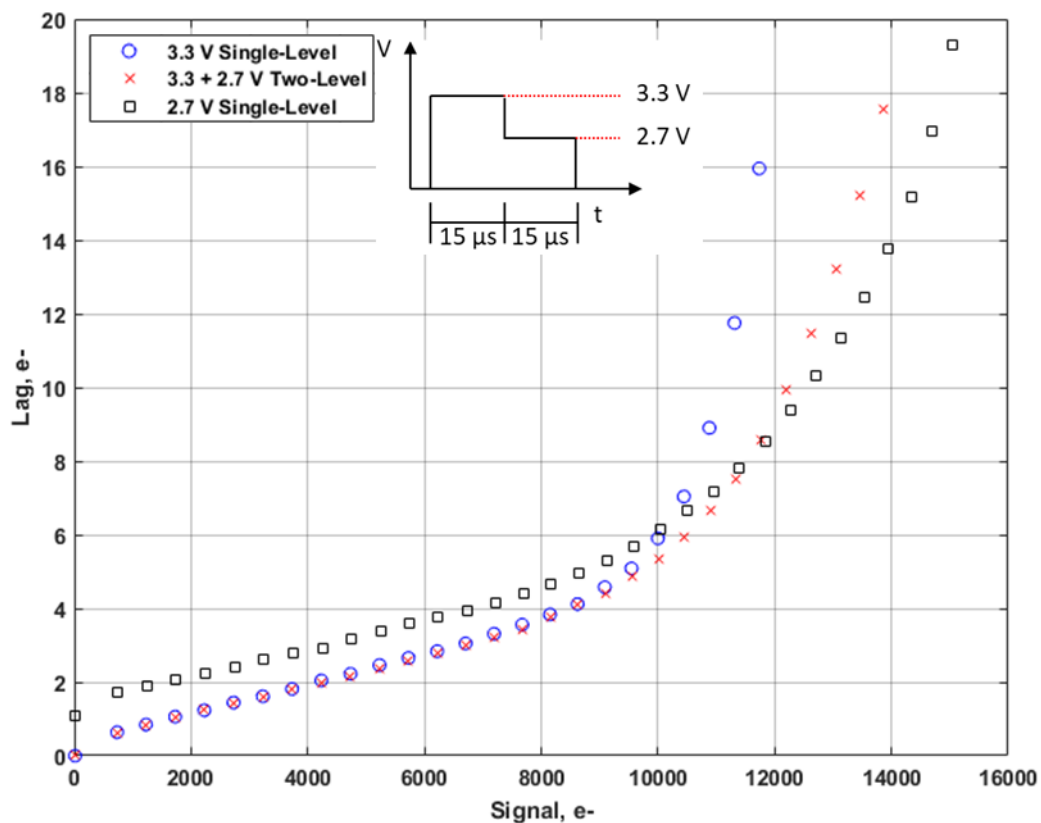


Figure 5-15: Image lag measured using a two-level transfer gate voltage regime, compared to a standard single voltage level. The crosses represent the two-level VTG measurements  $VTG_H = 3.3$  V,  $VTG_M = 2.7$  V, while the squares represent the lag measured at a single level  $VTG_H = 2.7$  V and the circles represent the lag measured at a single level  $VTG_H = 3.3$  V. The data shown is for a 30 μs long TG pulse, and for a two-level VTG at 15 μs per level, displayed in the inset.

Figure 5-15 shows the results of image lag measurements with two-level VTG implemented as shown in Figure 5-14. The graph shows a comparison between this and the standard single voltage charge transfer method. The two-level VTG method shows lag at low signal levels as being almost identical to that of the single level  $VTG_H = 3.3\text{ V}$ , and lower than the lag of the  $VTG_H = 2.7\text{ V}$ . At higher signal levels, the lag using two-level VTG remains much lower than that with single  $VTG_H = 3.3\text{ V}$  results, and is almost the same as the lag measured when using the single level  $VTG_H = 2.7\text{ V}$ . Tests were run at a number of combinations of high and medium voltages and the combination of  $3.3\text{ V}$  and  $2.7\text{ V}$  shown in Figure 5-15 was found to give the best results. Any values for  $VTG_M$  lower than  $2.7\text{ V}$  are likely too low to draw electrons from the photodiode to the floating diffusion. Any values of  $VTG_M$  higher than  $2.7\text{ V}$  are more susceptible to charge spillback.

### 5.9.2 Time Dependence

Using the value for  $VTG_H$  and  $VTG_M$  found in the previous section,  $3.3\text{ V}$  and  $2.7\text{ V}$  respectively, it is important to find out what optimal timing scheme is for each voltage. Tests were run to find the values for  $T_1$  and  $T_2$  from Figure 5-14 which gave the lowest values for image lag.

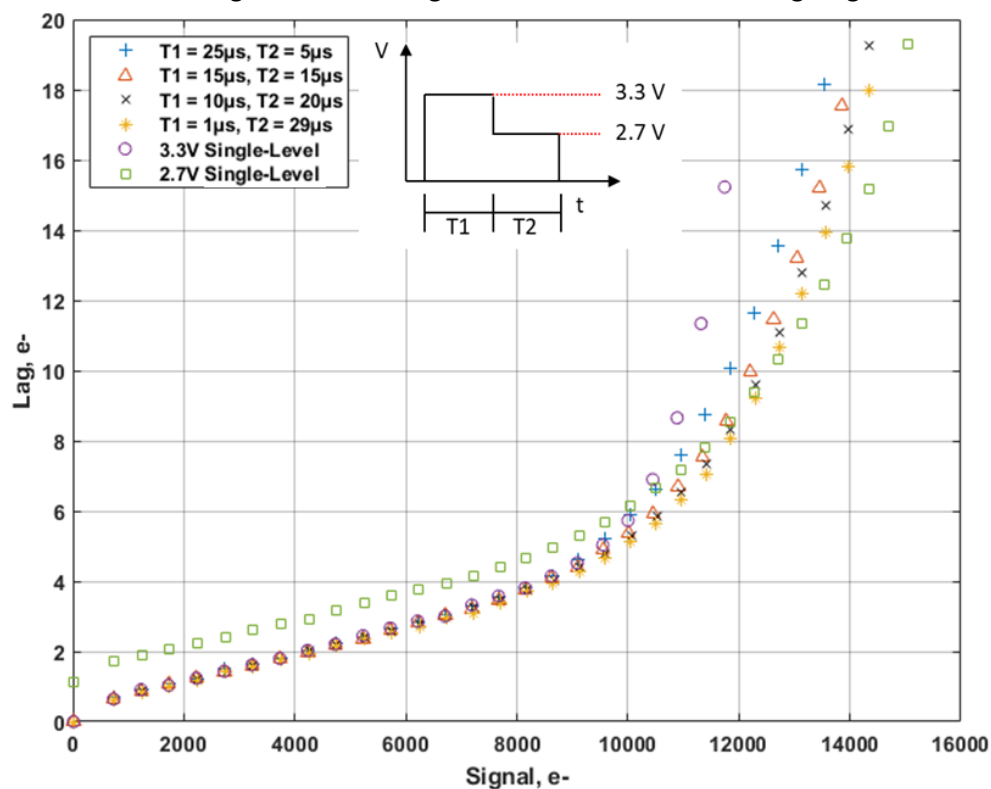


Figure 5-16: Image lag measured with varying timing of the two voltage levels  $VTG_H$  and  $VTG_M$  in comparison with a single level VTG. Total TG on time is  $30\mu\text{s}$  for all measurements, i.e.  $T_1 + T_2 = 30\mu\text{s}$ .

Figure 5-16 shows the results of the measurements where the times at VTG<sub>H</sub> and VTG<sub>M</sub> are non-equal, varying T1 and T2, but keeping the total transfer time the same. From these results, it can be seen that increasing the time of VTG<sub>M</sub> during readout leads to the best lag performance. As T2 increases beyond 5 µs the lag performance increases, and all offer lower lag than the standard 3.3 V at larger signal levels.

A longer T2 is thought to be preferable due to the short pulse of high voltage being able to pull across the majority of photogenerated electrons in a short time, and the longer middle voltage then allows electrons to drift into the FD, reducing spill-back.

## 5.10 Ramped Down VTG<sub>H</sub> Measurements

The final tests were run with an exponentially decaying VTG<sub>H</sub> instead of a fixed VTG<sub>M</sub>. The decay time was controlled by varying the resistor, as shown in Figure 5-13. The results of characterisation measurements of the RC circuit are shown in Table 5-1.

Resistance (kOhm)	Time to 1/e Volts (µs)	Time to 500mV (µs)
0	0.498	0.658
1	1.4582	2.7782
2	2.5382	5.0582
3	3.5782	7.2182
4	4.5982	9.582
5	5.6982	11.698
6	6.6982	13.898
7	7.7982	16.098
8	8.7982	18.098
9	9.7982	20.298
10	10.898	22.398
11	11.998	24.398

*Table 5-1: Decay rate of the voltage applied to the transfer gate during readout.*

The voltage  $V_{out}(t)$  at the output of an RC circuit after a given time  $t$  is:

$$V_{out}(t) = V_0 e^{-\frac{t}{RC}} \quad (5-3)$$

Where  $V_0$  is the initial voltage in volts,  $t$  is the time passed in seconds,  $R$  is the resistance in the circuit in ohms and  $C$  is the capacitance of the circuit in farads. The time constant  $\tau = RC$  is the time taken for the voltage to fall to  $1/e$  of its original value. Figure 5-17 shows oscilloscope traces of the output voltage decay with  $R = 1\text{ k}\Omega$  and  $10\text{ k}\Omega$ .

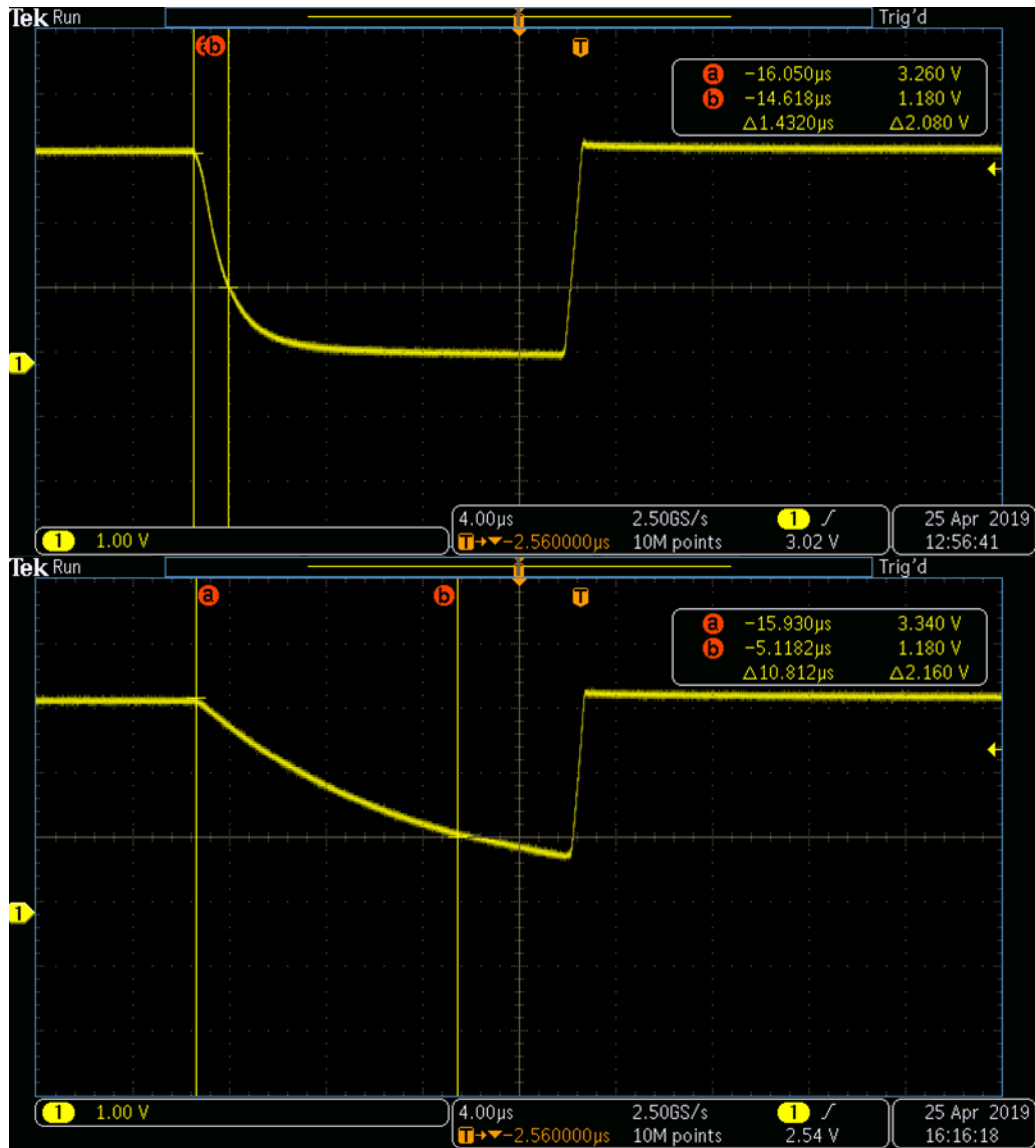


Figure 5-17: Comparison of the RC time constant to the resistance of the circuit. The top oscilloscope trace is taken with  $R = 1\text{ k}\Omega$ , the lower with  $R = 10\text{ k}\Omega$ .

With the discharge times known, it is possible to tune the circuit resistance to give different shaped voltage decays. Measurements were taken at varying decay rates and different T1 and T2 values.

It was found that instead of decaying to 0 V over the transfer period, the lag was at its lowest when VTG<sub>M</sub> was implemented as the final voltage for the RC circuit to decay to. This is because once the voltage applied to the transfer gate falls below  $\sim 2.7\text{ V}$ , the potential is no longer high enough to

draw electrons across to the floating diffusion and any time spent below this value is wasted. Results indicated that a larger resistance, therefore slower voltage decay, was optimal for reducing image lag.

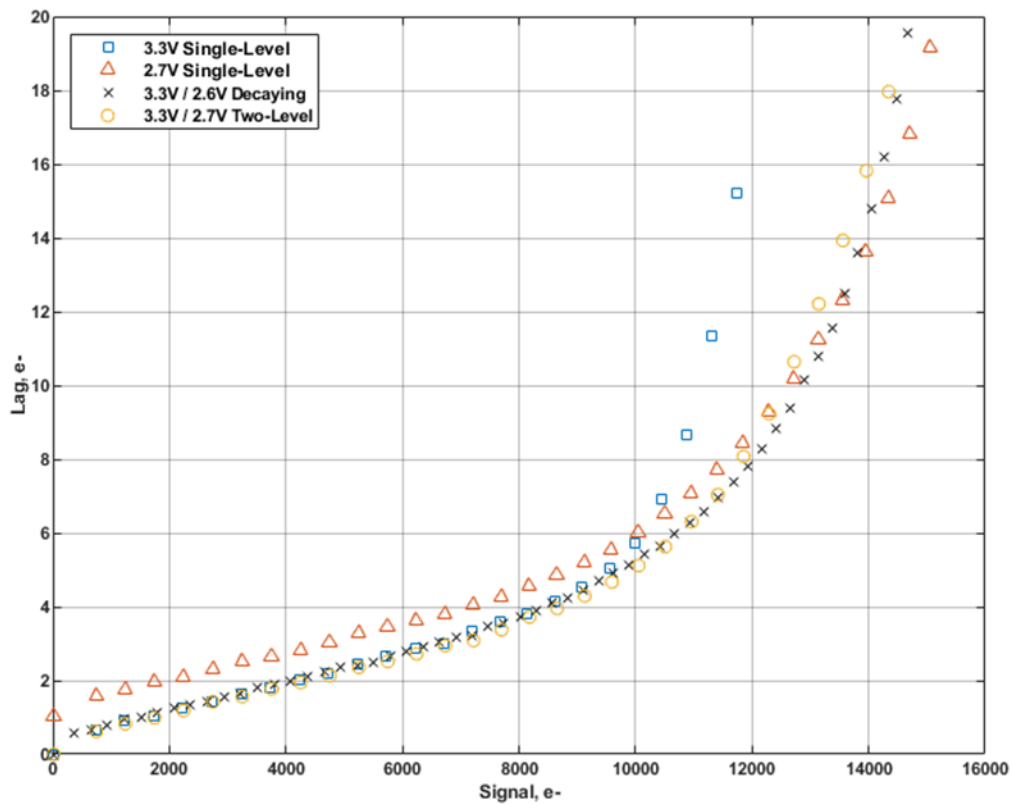


Figure 5-18: Lag measurements comparing all three methods – single level  $VTG_H$ , two-level  $VTG$  and a ramped down  $VTG_H$ . Both the two-level and decaying  $VTG_H$  exhibit the advantages of the two single-level  $VTG_H$  tests. In both multi-level tests  $T1 = 1 \mu s$  and  $T2 = 29 \mu s$ , with  $R = 10 k\Omega$  for the ramped down tests.

The operating parameters that gave the lowest image lag were found to be  $VTG_H = 3.3 V$ ,  $VTG_M = 2.6 V$ ,  $T1 = 1 \mu s$  and  $T2 = 29 \mu s$ .  $VTG_M$  is slightly lower here than in the two-level regime, most likely due to the voltage decay being asymptotic to the minimum voltage, so it never fully reaches 2.6 V. Comparisons between normal readout, two-level and ramped down  $VTG_H$  results are shown in Figure 5-18.

The ramped down transfer gate voltage and the two-level regime result in very similar lag, although the decaying voltage gives marginally better results. Both methods combine the advantages of the high and low single-level transfer gate regimes.



## 5.11 Conclusions

Characterisation of image lag on this device with regard to transfer gate voltage and transfer time provided a foundation on which to base spillback reduction techniques.

Through measurements of the image lag as a function of both the  $VTG_H$  and the potential at the floating diffusion after reset, results obtained support the theory that charge spillback dominates image lag at higher signal levels. By showing that a high transfer gate voltage or a lower reset voltage decreases the signal at which spillback dominates, it can be seen that these parameters are important factors to consider when trying to reduce the image lag. Whilst a high voltage on the transfer gate may be beneficial at small signals in low light conditions, a lower voltage may be more pertinent in images captured with more light or longer integration times. The single level transfer results show that using a high voltage gives between a 50% improvement to lag at very low signal levels, to a 15% improvement at signal levels just before spillback occurs. Once spillback has occurred in the high voltage regime, the lower voltages still allow for  $\sim 4000$  signal electrons to be accumulated before spillback dominates.

The two-level transfer gate technique has shown that the effects of charge spill-back can be reduced by altering the TG potential during transfer. The change allows electrons under the gate to more favourably spill into the floating diffusion and therefore decrease the risk of them returning to the photodiode once the gate is turned off. The results have shown that with two-level transfer gate voltage, the benefits of both are seen, namely lower lag at both small and large signals. It was found that a short  $VTH_H$ , 1  $\mu s$  in this case, followed by a long  $VTG_M$ , 29  $\mu s$ , gives the lowest values for lag.

The decaying  $VTG_H$  results showed a slight reduction in lag when compared to the two-level VTG. As with the two-level VTG, a short  $VTG_H$  and a long  $VTG_M$  gave the best results. A large resistance is also more favourable due to the slow decay of the voltage meaning that the threshold voltage of the transfer gate is not reached during the transfer time. Ideally this method of controlling the transfer

voltage would be used in every situation to minimise the lag, although it is harder to implement than the two-level regime as it requires characterisation of the RC circuit decay time.

The proposed method has the advantage that it is easy to implement, with the majority of current CMOS sensors able to benefit from this with just a few hardware or software changes that are quick to make. There is no need to redesign or manufacture new chips with doping gradients or novel transfer gate shapes in order to reduce lag.

## 5.12 References

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## 6 Non-Uniformity and PSF in CMOS Image Sensors

### 6.1 Introduction

As described in Chapter 4, one of the unique properties of the BSB1 devices is the capability of being reverse biased. This allows the device to be fully depleted, allowing thicker devices, thus improving the Modulation Transfer Function (MTF) and decreasing lateral charge diffusion.

This chapter details an investigation into pixel non-uniformity and PSF of the BSB CMOS image sensors.

The PSF of the BSB devices is of great interest as a decrease in the spread of a point source is one of the main objectives in the design of the devices. Measurements of the wavelength dependence of the PSF is investigated, as well as the dependence on the reverse bias applied to the sensor. The dependencies are determined via two methods – stationary spot method and the virtual knife edge (VKE) method – with results presented for each.

### 6.2 Theory

#### 6.2.1 Photo-Response Non-Uniformity

The photo-response non-uniformity of a device is a measure of how the measured signal changes between pixels exposed to the same number of photons [1]. Ideally, the pixels would all have identical signal levels when read out. Minor inconsistencies which arise during manufacture can lead to different signal levels being measured by each pixel.

The pixel features, such as the photodiode, floating diffusion and transfer gate, are formed by implanting dopants into the silicon of the sensor. If the masks used to control the areas in which these implantations occur are misaligned, the areas will be different sizes to the ones expected. The size of the photodiode affects the full well capacity, as well as photosensitive area. The size of the floating diffusion has a direct impact on its capacitance and therefore the output voltage of the pixel.

The transfer gate size and area affect the charge transfer, and other gate sizes will impact the readout chain. These small variations will lead to different signal values from pixel to pixel.

CCDs do not suffer from photo-response non-uniformity on the same scale as CMOS sensors as all pixels share a common output. This leads to much lower measured PRNU in CCDs.

### 6.2.2 Intra-Pixel Non-Uniformity

Intra-pixel non-uniformity is a measure of how different areas within the pixel respond to light.

Whilst the readout electronics of a CMOS sensor are still sensitive to incoming photons, any electrons generated in these regions will not be measured, as they are not able to be drawn to the photodiode to be sampled. This can result in areas of a pixel less sensitive to light when measuring sub-pixel point sources.

In front-side illuminated sensors, the metallisation can reflect incoming light, causing a loss of signal in these areas. This results in what is known as fill-factor, a metric which describes what proportion of the sensor is sensitive to light [2]. A method for increasing the apparent fill-factor of a sensor is through the use of micro-lenses to focus the light on the light sensitive parts of each pixel [3].

### 6.2.3 Point Spread Function

The Point Spread Function (PSF) [4] describes the lateral diffusion of photogenerated charge within a sensor. The spreading of charge results in a blurring of light sources in the final image, as electrons generated in one pixel may travel to the next before being captured by the photodiode. Knowledge of the PSF of a sensor is useful as it can be used to reverse the blurring of images through deconvolution.

As discussed in Chapter 4 different wavelengths of light have different absorption depths within silicon. This leads to electrons being generated at different depths in a sensor, not necessarily within the depletion region. Any charge generated in the field free regions of the sensor can spread into neighbouring pixels, where they can be drawn into the photodiode and read in that pixel instead.

To reduce the effect of charge spreading, the sensor must be fully depleted, so that the depletion regions extend to the back side of the device, leaving no field free areas. Using the equation from Chapter 2, given again here as Equation (6-1), the depletion depth  $W$  for a sensor is

$$W = \sqrt{\frac{2\epsilon_{si}\epsilon_0(V_{pin} + V_r)}{qN_A}} \quad (6-1)$$

Where  $V_{pin}$  is the pinning voltage of the pinned photodiode and  $V_r$  is the reverse bias applied to the sensor. As can be seen, increasing either of these will increase the depth of the depletion region in the pixels. Using this and the thickness of the sensor, the reverse voltage needed to fully deplete the sensor can be calculated. Increasing the voltage past the point of full depletion results in over-depletion of the pixel, which is advantageous [5]. Figure 6-1 shows the potentials through a device with under-depletion, full depletion and over-depletion. Over-depletion raises the electric field at the surface of the sensor above zero, to  $E_{min}$ , increasing the chance that an electron generated there will be collected quickly into the photodiode.

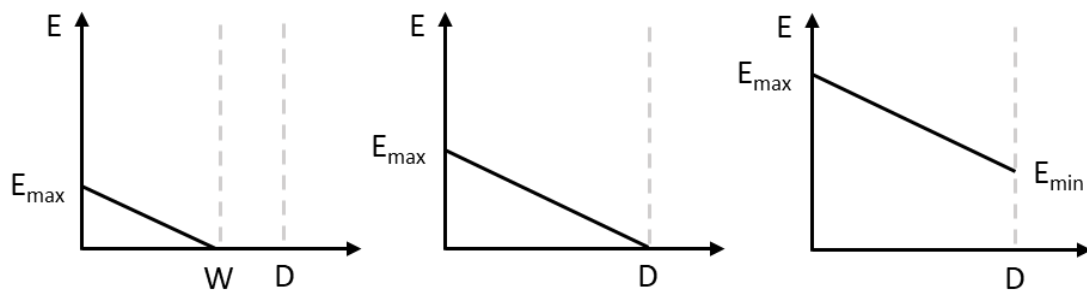


Figure 6-1: Under-depletion (left) full depletion (middle) and over-depletion (right) of a sensor.  $W$  represents the depletion depth, and  $D$  is the depth of the sensor. For full and over-depletion,  $W = D$ .  $E$  represents the electric field.

The depth at which photons are absorbed is described by the Beer-Lambert law, which states that the remaining intensity of light,  $I$ , after travelling through a material of thickness  $z$  is

$$I(z) = I_0 e^{-\alpha(\lambda)z} \quad (6-2)$$

Where  $I_0$  is the initial intensity and  $\alpha$  is the wavelength dependent absorption coefficient.

The probability of an electron having been absorbed after a depth  $z$  is then simply

$$P(z) = 1 - e^{-\alpha(\lambda)z} \quad (6-3)$$

The absorption coefficient,  $\alpha$ , is given as

$$\alpha = \frac{4\pi k}{\lambda} \quad (6-4)$$

Where  $k$  is the extinction coefficient and  $\lambda$  is the wavelength.

The inverse of the absorption coefficient is the absorption depth shown in Figure 6-2.

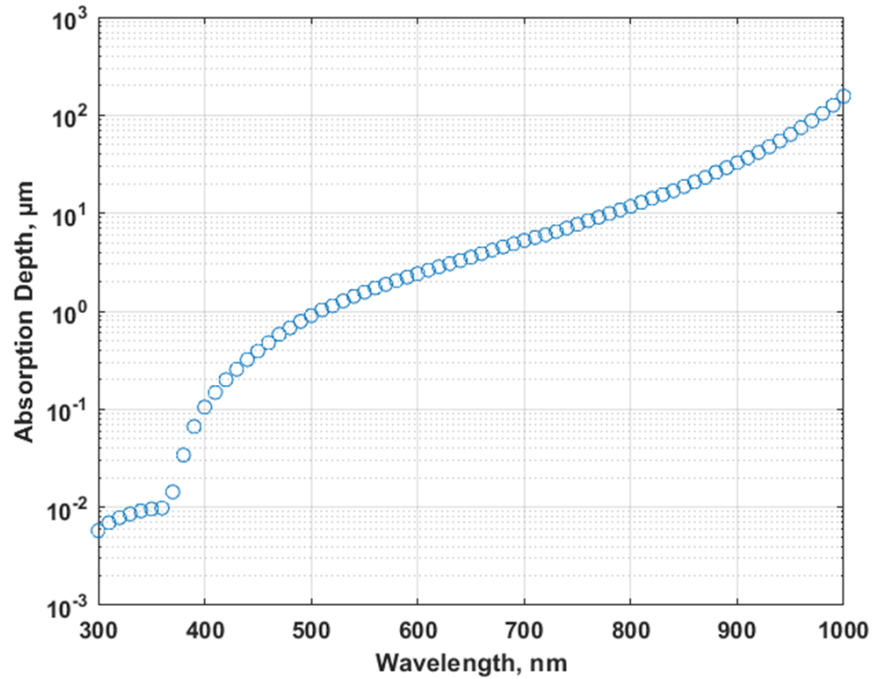


Figure 6-2: Absorption depth of silicon as a function of wavelength. Data taken from [6].

The absorption depth of a material is defined as the depth at which  $I$  has dropped to  $1/e$  of the initial value  $I_0$ .

Calculating the depletion depth of a device and knowing the absorption depth of the wavelength of light being measured can help determine the scale of lateral charge diffusion.



## 6.3 Experimental Details

### 6.3.1 Experimental Setup

All experiments were run using the same camera circuitry and software as described in Chapter 4.

The camera was placed into a large dark box in order to accommodate the necessary optics and mechanical components required to create and move a point source relative to the sensor.

The point source is generated using the optics depicted in Figure 6-3.

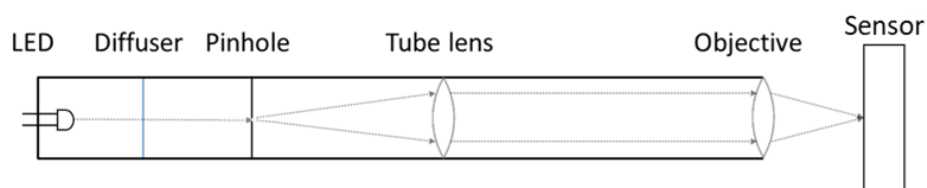


Figure 6-3: Diagrammatic representation of the optics used for non-uniformity and PSF tests.

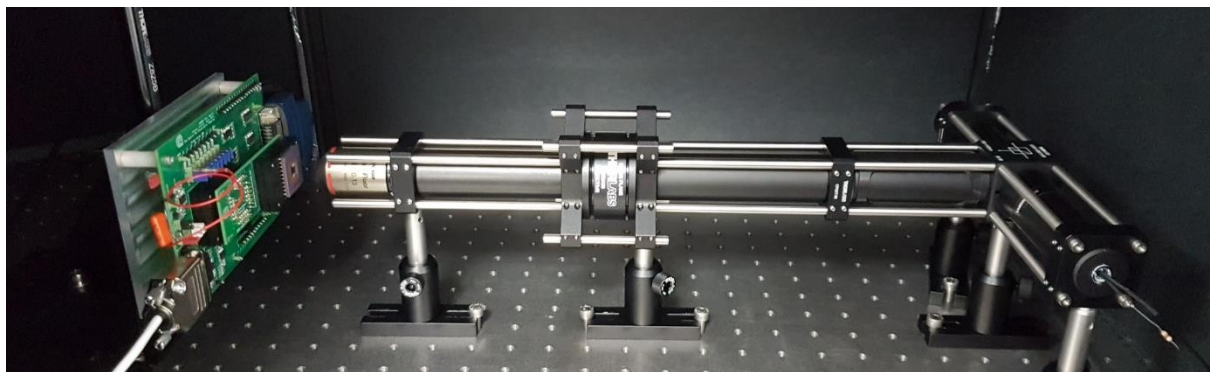


Figure 6-4: Photograph of the optical and electrical apparatus used for non-uniformity and PSF tests.

The light source used for the measurements were bright LEDs, connected to an external power supply. The LEDs were mounted in a threaded mount which allowed for easy switching without disturbing the rest of the optical setup and also guarantees good alignment of the output parallel to the desired path. The power supply could not be controlled via software, so the LED was on continuously with the brightness set by changing the current manually. The LEDs used are shown in Table 6-1.

LED Part Number	Typical Wavelength (nm)	Colour
C503B-BCS	470	Green
C503B-GCS	527	Blue
C503B-RCS	624	Red
SFH 4557	850	NIR
SFH 4547	940	NIR

*Table 6-1: Specifications for the LEDs used in the non-uniformity and PSF measurements.*

The range of LEDs was chosen to probe the effects of different absorption depths of photons in silicon sensors. This is discussed later in Section 6.6.1. The linearity of the LEDs used was not evaluated or factored in to any measurements or results, which may be an important consideration in any future work.

The light from the LED passes down the tube, through a ground glass diffuser which flattens the field of light. From there the light passes through a pinhole, of which there are three sizes – 5, 25 and 50  $\mu\text{m}$ . From the pinhole, the light spreads outwards in a cone shape towards a collimating tube lens. This collimates the light, making the waves run parallel to each other and the tube. The collimated light then enters a microscope objective with a magnification factor of 5. This creates a spot of light on the sensor which is, depending on the pinhole used, either 1, 5 or 10  $\mu\text{m}$  across.

The sensor is mounted on the PCB, which was mounted on a metal frame to avoid any bending of the board. This in turn was mounted on a 3-axis x-y-z translation stage. Each stage is capable of independent movement, have a range of movement of 25 mm and a movement resolution of 70 nm. The sensor is oriented such that movement in the x-axis corresponds to moving along a row of pixels, the y-axis corresponds to columns and the z-axis is orthogonal to the chip face, shown in Figure 6-5.

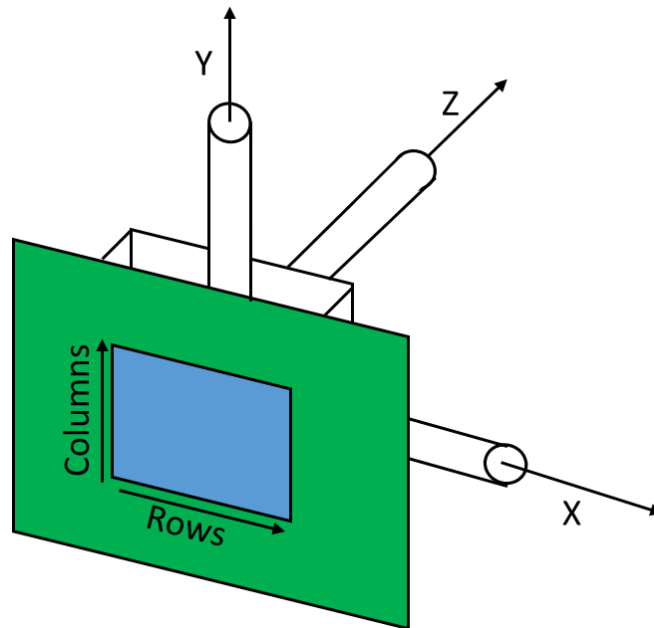


Figure 6-5: Diagram illustrating the movement axes of the translation stage and the movement directions relative to the sensor. Green represents the control board with blue the sensor itself.

The stages are each connected to an external controller, which power and interface with the motors, sending move commands and receiving positional information. These cubes are connected to a hub which allows control over all three via a single USB connection to the PC. The movement and timing of the motors was done in LabVIEW. This was chosen because it could be integrated into the programming for running the camera system, allowing feedback between the image capturing and stage movement.

## 6.4 Optical Alignment

### 6.4.1 Spot Focussing

In order to carry out measurements on PSF and non-uniformity, a well-focussed point source is essential. Proper focussing ensures the spot of light is the expected diameter. Focussing must be the first test run on the optical system in order to allow all other alignment tests and any measurements.

To focus the light, first the sensor must be set to continuously take images, preferably at a high frame rate. This is so that the spot can be found and positioned on a suitable pixel. The sensor is moved in the z-axis whilst constantly monitoring the signal level in the chosen pixel. When the z-axis position is found that gives the maximum signal output, a focussing algorithm is run. This moves the sensor  $-40\text{ }\mu\text{m}$  in the z direction and takes 100 images. The mean value for each pixel is calculated across all the images, and a single image is created from the results and saved. The sensor is then moved  $+1\text{ }\mu\text{m}$  in the z direction and another 100 images taken. This process is repeated until the sensor reaches  $+40\text{ }\mu\text{m}$  relative to the starting point, resulting in 80 averaged images. The signal in the chosen pixel is then taken in each of the images and plotted against the absolute displacement of the z-axis translation stage. An example of the graph produced is shown in Figure 6-6. The point at which the signal is greatest is taken as the point at which the light is properly focussed.

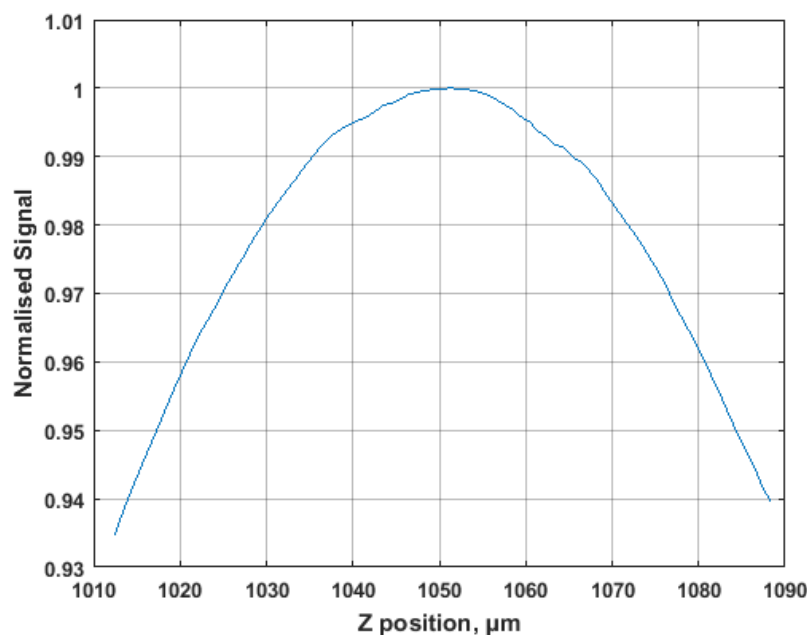


Figure 6-6: An example of a graph produced when focussing the beam of light. In this case, the focus position for the z-axis is located at  $1051\text{ }\mu\text{m}$ .

This procedure must be repeated for each wavelength of light due to chromatic aberration caused by the lenses used [7]. As well as this, the focussing program is run each time the pinhole is changed and at the start of each day that tests were run to account for any temperature changes that may occur overnight.

### 6.4.2 X-Y Alignment

The sensor is mounted in a ZIF socket, onto a PCB which is mounted on a plate that is bolted to a set of 3 translation stages. Each of these mountings are manufactured to certain tolerances which are unknown to the end user. Since the sensor and translation stages have these tolerances between them, it can lead to the sensor and stage axes being slightly misaligned. This means that movement in the x-axis of the translation stage will translate to not only movement in the row direction of the sensor, but also the column and move the chip closer or further from the optics.

To check the x-y alignment of the chip, the optics are first focussed. X-axis alignment was tested by moving the point source from Array 0 of the 10  $\mu\text{m}$  pixels to Array 3. These two arrays are separated by 1100  $\mu\text{m}$ , shown in Figure 6-7, far greater than the 80  $\mu\text{m}$  distance needed for the measurements.

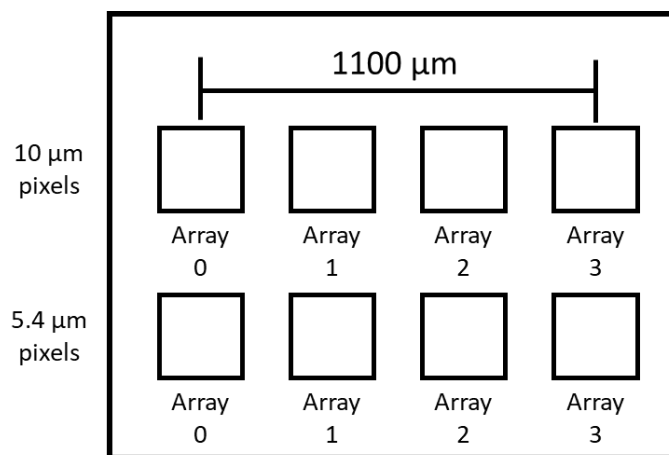


Figure 6-7: Layout of the eight arrays on the chip, showing the distance across which the alignment is measured.

Firstly, the focussed spot was centred in a pixel in Array 0, at coordinate  $(x, y)$ . This is done by observing the signal in the pixel and its surrounding pixels, moving the point source until the signal of pixels  $(x, y+1)$  and  $(x, y-1)$  were equal. The same is done in the x direction. Using the translation stages, the point source is then shifted to Array 3, a distance of  $\Delta x$ , and the point source centred on a pixel in the same row as the one chosen in Array 0. The difference between the y-axis displacements,  $\Delta y$ , is then calculated for the two arrays. Dividing  $\Delta y$  by  $\Delta x$  gives a correction factor in the y direction needed per micron of movement in the x direction.

After some initial alignment measurements and small adjustments, over  $\Delta x = 1100 \mu\text{m}$  displacement in the x direction, the displacement in the y direction was found to be  $\Delta y = 3 \mu\text{m}$ . This gives a correction factor of  $0.0027 \mu\text{m}$  in the y-axis for each micron moved in the x-axis, or  $0.027 \mu\text{m}$  per pixel. Over the  $80 \mu\text{m}$  distance travelled to perform the tests, this equates to a total correction of  $0.216 \mu\text{m}$ , or one fiftieth of a pixel pitch. Due to the small scale of this correction factor, and the fact that it is only three times the resolution of the translation stages, the decision was made to not implement any corrections during the measurements.

A similar method was employed for the y-axis alignment. Due to the physical layout of the arrays, alignment in the y direction could only be tested over a single array. To do this, a pixel in the second row was chosen as the starting point and a pixel in the penultimate row chosen as the end point. As with the x direction alignment, the point source was centred, moved and re-centred. The change in x displacement was divided by the change in y displacement and a similar correction factor was found,  $0.196 \mu\text{m}$  over eight pixels. This is expected as the x- and y-axis alignment are intrinsically linked.

### 6.4.3 Z Alignment

When moving the point source across the sensor it is important that the light remains in focus for the duration of the experiment. For this, each pixel on the sensor must be the same distance away from the light source i.e. the sensor must be flat.

To verify the z-axis alignment, a similar method to the x-axis alignment is used. Firstly, the point source is focussed on a pixel in Array 0, and the z-axis displacement value recorded. The sensor is then moved so that the light is on a pixel in Array 3. The focussing program is then run again, and the z-axis displacement recorded. The correction factor for the z-axis was found to be below the resolution of the translation stages, so no corrections were performed during the tests.

## 6.5 Photo-Response Non-Uniformity

This section describes measurements performed to examine the sensitivity of individual pixels to a point source of light. The results show the uniformity of the sensor as a whole, pixel to pixel, as well as within individual pixels.

### 6.5.1 Inter-Pixel Non-Uniformity

To probe the inter-pixel non-uniformity, the point source of light is scanned across a row of pixels at a time. After focussing, the light is centred on the starting pixel, and the LED current adjusted to 1000 ADU, well within the linear range of the device. The point source then moved across a group of eight pixels in steps of 400 nm. At each location, 100 images are taken, and the mean of these images saved. For each mean image, the total signal in each of the eight pixels is calculated, minus a dark frame, and plotted against the displacement of the translation stage. All pixels are plotted individually on the same axes.

#### 6.5.1.1 Front-side Illuminated Device

A line scan of a front-side illuminated variant of the devices is shown in Figure 6-8. The pixel-to-pixel uniformity is 98% in the group of pixels measured. The maximum signal generation occurs when the spot of light is focussed in the centre of each pixel, where the PPD is located. Similar results were found for other rows measured, with the maximum non-uniformity found to be 2%.

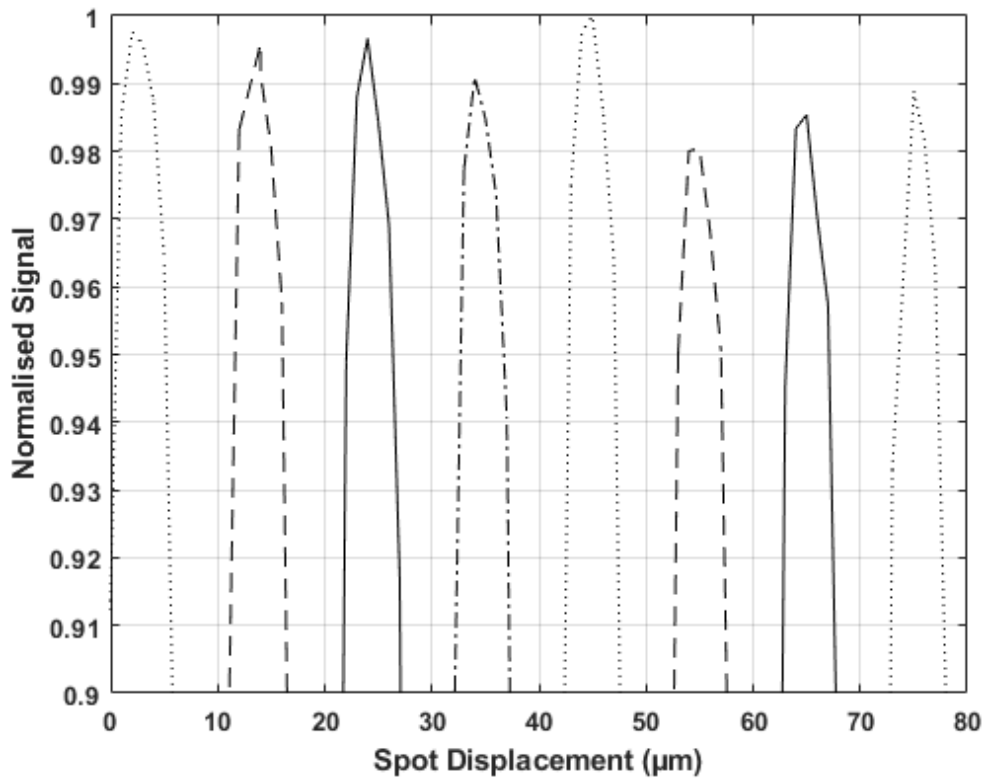


Figure 6-8: Inter-pixel non-uniformity measured with a 470 nm source, measured across the eighth row. Edges of the pixels align with the grid, with the centres found halfway between grid lines.

#### 6.5.1.2 Back-side Illuminated Device

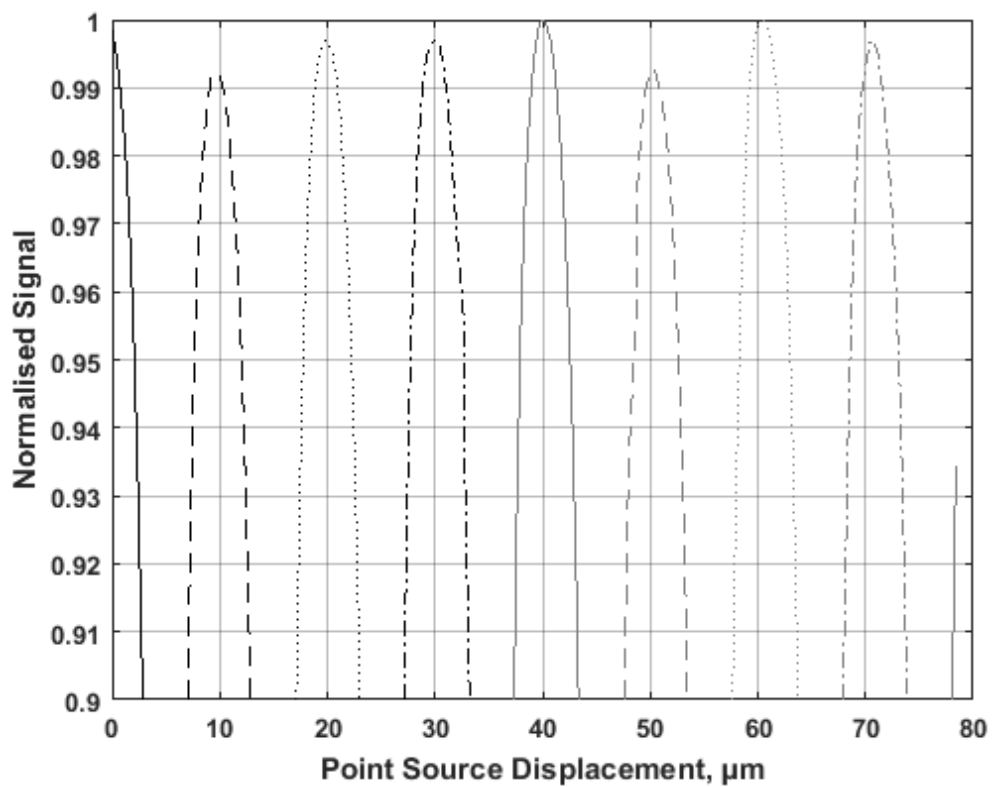


Figure 6-9: Inter-pixel non-uniformity measured with 470 nm light source, measured across the eighth row. The centre of the pixel is in line with the grid markers at each multiple of 10  $\mu\text{m}$ .



A line scan of eight pixels, with a 1  $\mu\text{m}$  point source at  $\lambda = 470 \text{ nm}$ , is shown in Figure 6-9. The centre of each pixel scanned aligns with the grid markers at each multiple of 10  $\mu\text{m}$ . From this graph, it can be seen that the sensor is quite uniform from pixel to pixel, with the difference between maximum signal values between pixels is  $< 1\%$ . The maximum signal values occur when the point source is located in the centre of the pixel, which is as expected as it is where the PPD is located and is the area with the highest electric field.

The results for the inter-pixel non-uniformity are very similar for all wavelengths of light used for these tests. Figure 6-10 shows the results for  $\lambda = 940 \text{ nm}$ . The difference between the peak signal values in the centre of each pixel is  $< 1\%$ , indicating that the wavelength of the light incident on the sensor has a negligible effect on the sensitivity to light on a pixel-by-pixel basis.

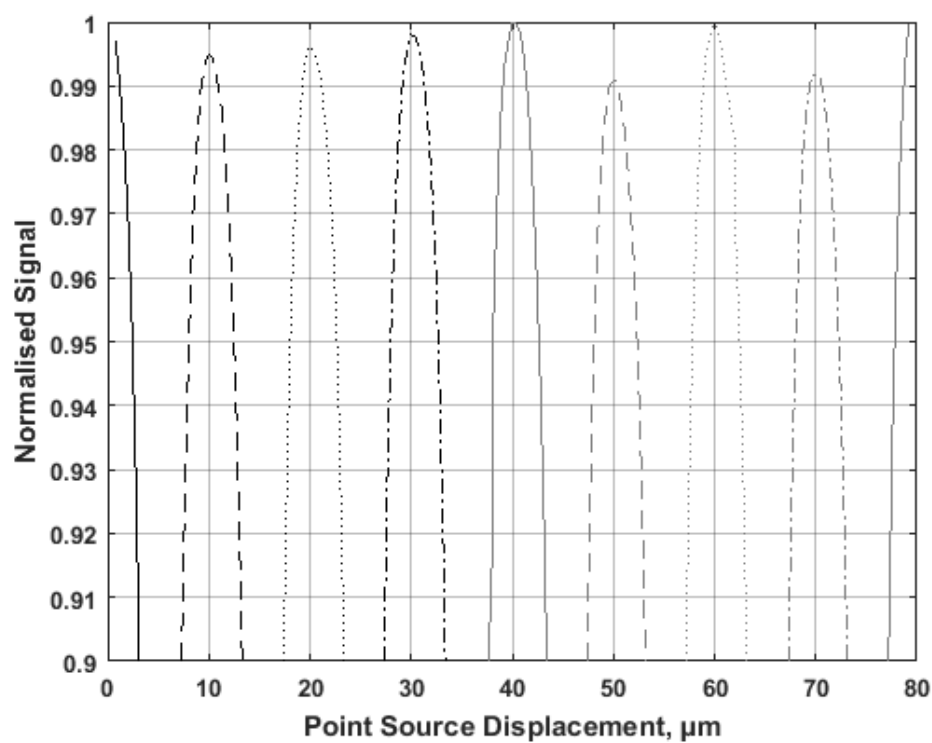


Figure 6-10: Inter-pixel non-uniformity measured with a 940 nm light source, measured across the eighth row. The centre of the pixel is in line with the grid markers at each multiple of 10  $\mu\text{m}$ .

After scanning multiple rows and columns, avoiding hot pixels, the non-uniformity was found to be < 1% across the device using this method. A comparison of all wavelengths is shown in Figure 6-11. No significant difference is found between any of the wavelengths with regards to photo-response non-uniformity.

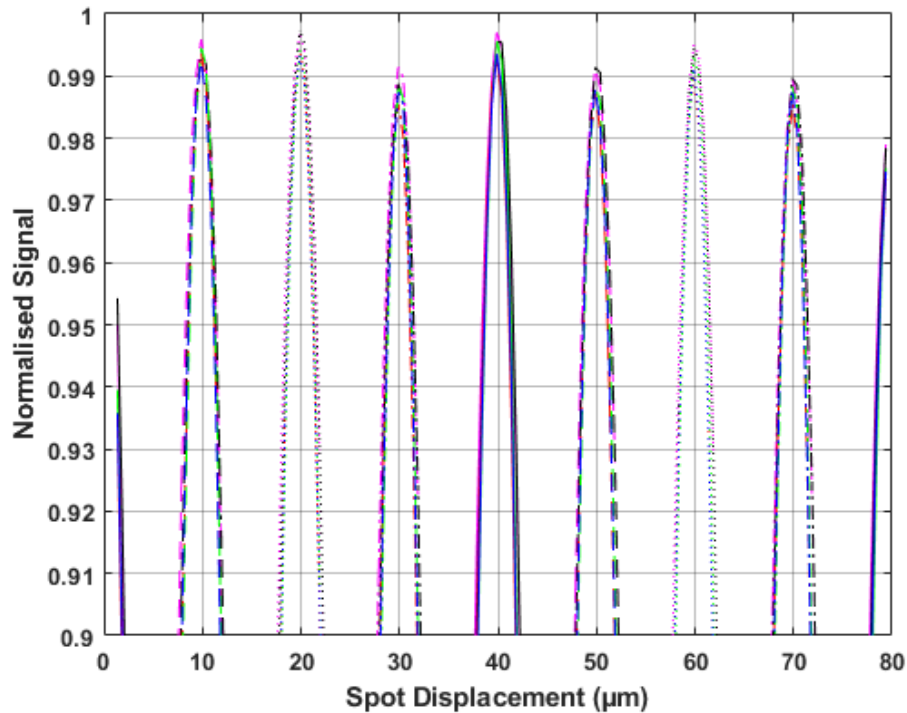


Figure 6-11: Comparison of photo-response non-uniformity at all five wavelengths used.

## 6.6 Intra-Pixel Non-Uniformity

### 6.6.1 Line Scanning

Measuring intra-pixel non-uniformity can be done using the same method and data as inter-pixel non-uniformity. In this method, as well as summing the signal in each individual pixel, the total signal in all eight pixels scanned is summed together at each point, giving the total signal in all of the pixels combined. As the spot is scanned across, the total signal should remain constant if there is no loss of signal anywhere within the pixel.

Figure 6-12 shows a line scan of eight pixels at  $\lambda = 470$  nm. It contains the same data as Figure 6-9, but with the total signal in all eight pixels added. In this figure, the same trend can be seen in the peaks as in the previous one. In an ideal sensor, the sensor response would remain constant at a value of 1 for the normalised signal as the point source is moved from pixel to pixel. Summing all of

the signal in the row accounts for when the signal is shared between more than one pixel. The data shows a drop in signal level at shorter wavelengths when the point source is on or near a pixel boundary, up to 1.6% in the most extreme case. Since the readout circuitry is located in the column direction, and these scans are in the row direction, the loss of signal cannot be attributed to it.

One explanation for this is that the pixels can share charge to the neighbouring rows via the DDE.

The DDE is a mesh structure which surrounds the pixels, which has its own depletion region. If electrons fall into this depletion region, they may travel to the next pixel.

Figure 6-14 shows results from the same method performed with light at  $\lambda = 940 \text{ nm}$ .

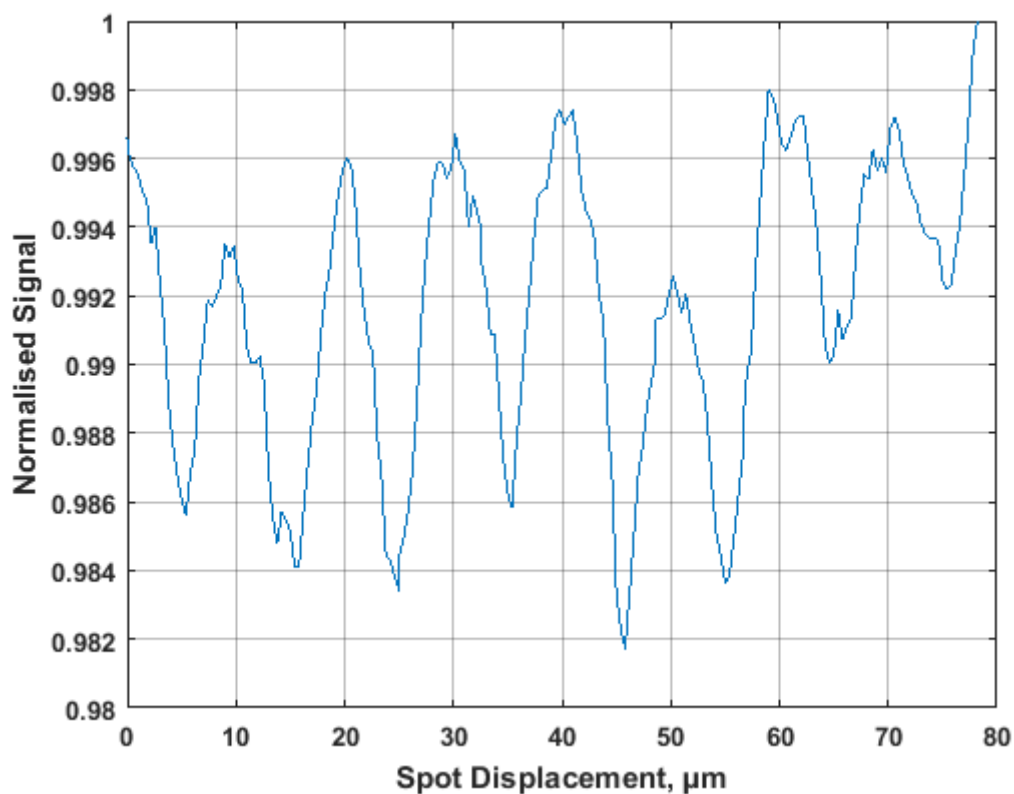


Figure 6-12: Line scan of 8 pixels with the total signal in all pixels summed together at  $\lambda = 470 \text{ nm}$ . The centre of each pixel is aligned with the grid markers at multiples of  $10 \mu\text{m}$ .

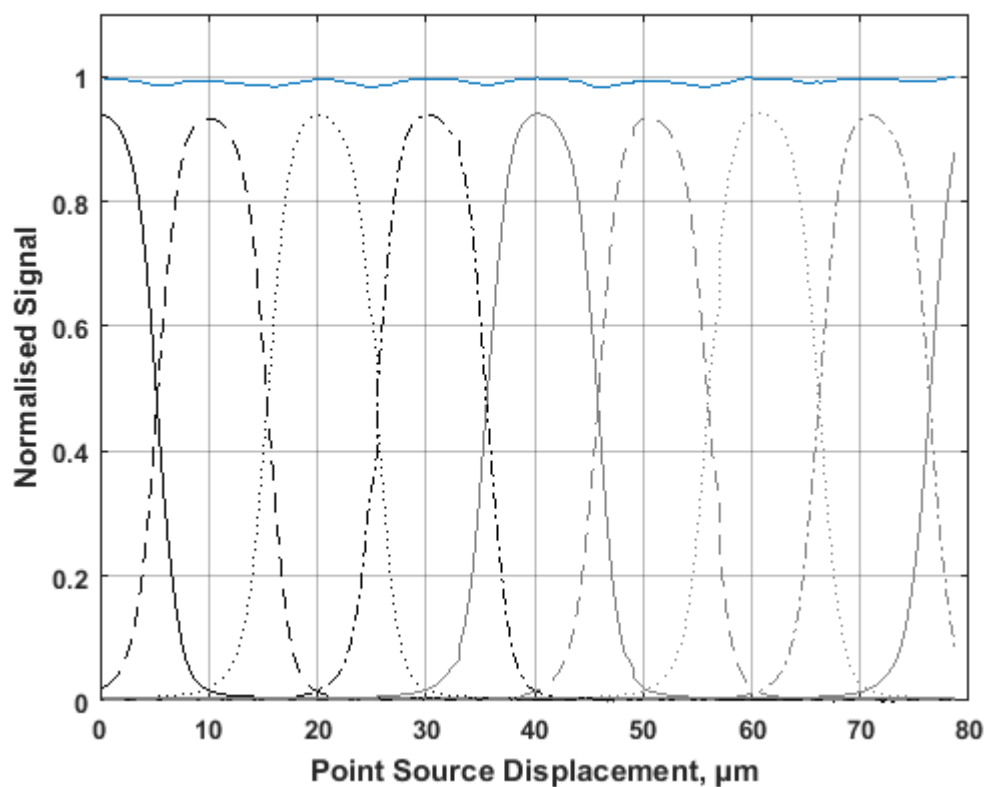


Figure 6-13: Line scan of 8 pixels at  $\lambda = 470 \text{ nm}$  with both individual pixel signal values and total signal represented.

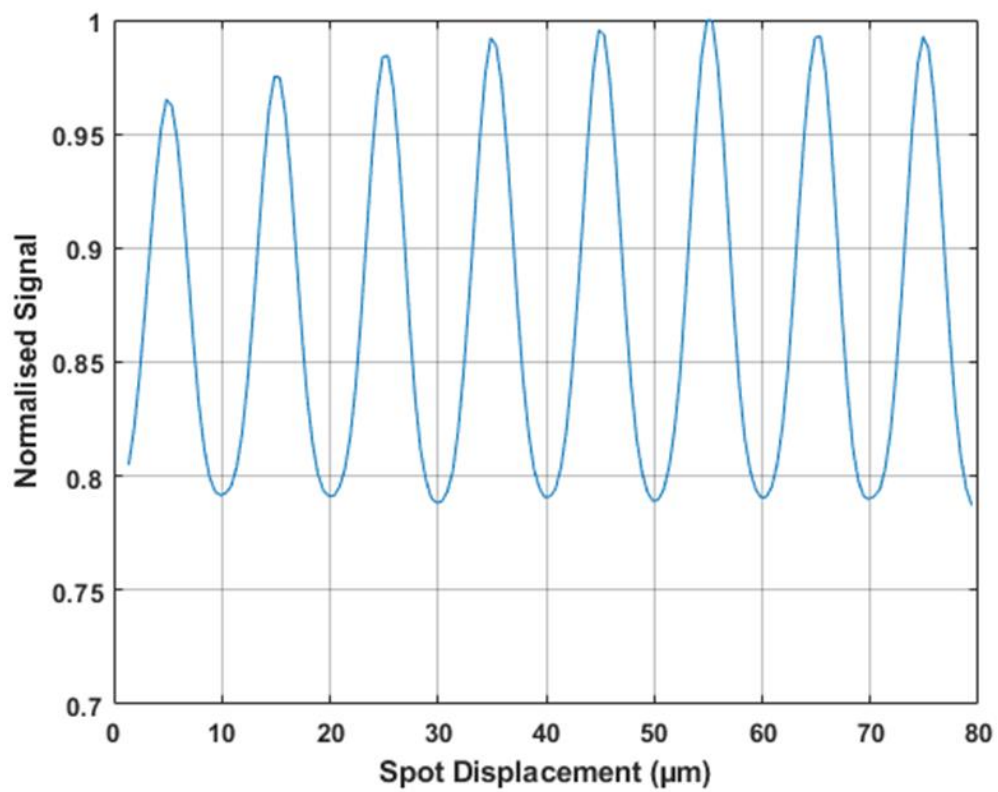


Figure 6-14: Line scan of 8 pixels with the total signal in all pixels summed together at  $\lambda = 940$  nm. The centre of each pixel is aligned with the grid markers at multiples of  $10\ \mu\text{m}$ .

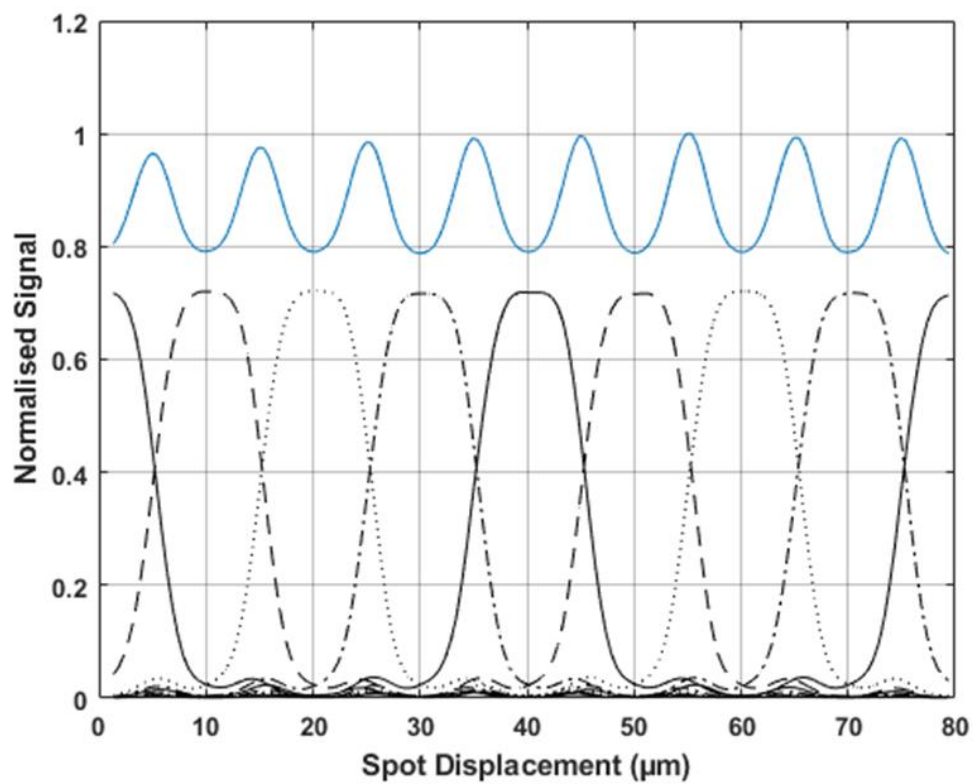


Figure 6-15: Line scan of 8 pixels at  $\lambda = 940$  nm with both individual pixel signal values and total signal represented.

The results for the longer wavelengths show a dramatic difference in intra-pixel non-uniformity to those of the shorter wavelengths. In this case, the greatest difference between maximum and minimum is 22%. The implications of this are that if a point source was measured in two separate areas of the pixel, the resulting signal could vary up to this amount. In the case of an astronomical measurements, this discrepancy could lead to miscalculations of the apparent magnitude of a measured star.

As well as the increased magnitude of the non-uniformity of the signal, the shape of the graph is inverted. For shorter wavelengths, the maxima of the signal are located in the centre of the pixel, when the point source is directed onto the PPD. In the case of the longer wavelengths, the minima are located when the point source is on the PPD, and the maxima are located at the pixel boundaries, shown in Figure 6-16. This inversion is due to the incident light being reflected off the metal tracks on the front of the sensor.

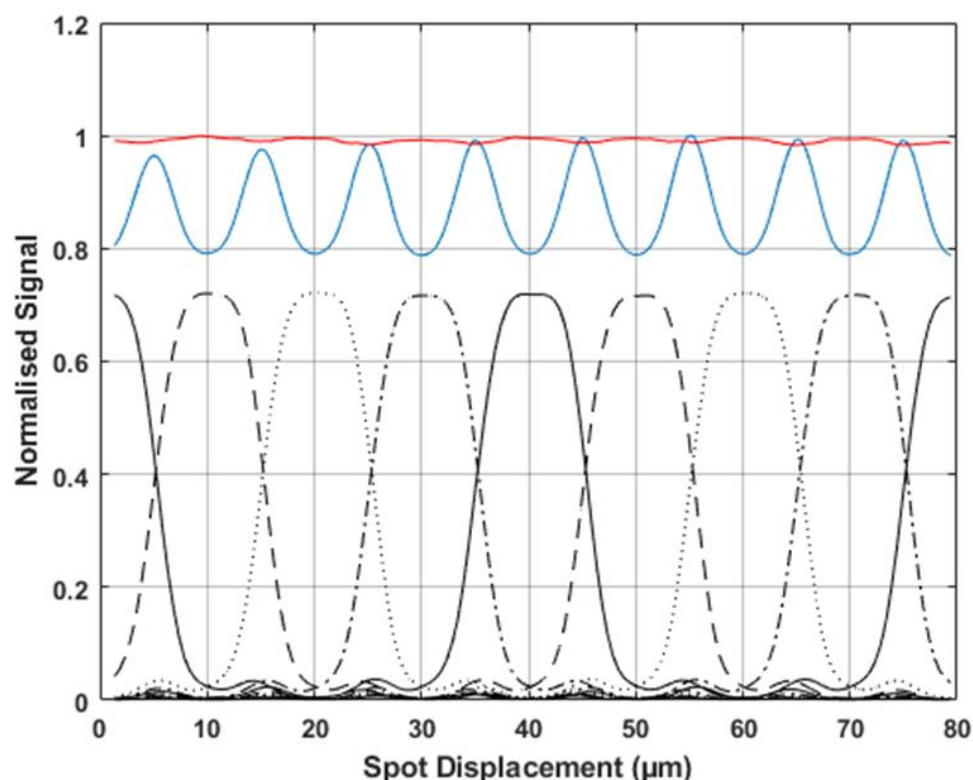


Figure 6-16: Comparison of total signal in all eight pixels at 470 nm (red) and 940 nm (blue) alongside the signal in each pixel at 940 nm. Maxima for total signal at 470 nm occurs at pixel peak signal, whereas maxima for signal peaks at 940 nm occurs at pixel boundaries.

Figure 6-2 shows the absorption depth of silicon at 300K. The data shows that the absorption depth for light below  $\lambda = 800$  nm is shorter than the thickness of the sensor, 12  $\mu\text{m}$ . This means that at  $\lambda = 800$  nm, ~74% of light is absorbed by the silicon. As the absorption depth increases, the percentage of light generating an electron within the sensor decreases exponentially.

At  $\lambda = 940$  nm, the absorption depth is 54  $\mu\text{m}$ , meaning that over the 12  $\mu\text{m}$  thickness of the device, only a 19.7% of photons will be absorbed. When the point source is over the PPD, the unabsorbed photons will pass through the front of the sensor and will not contribute to any further signal. When the point source is over the metal tracks, it has a chance to be reflected back into the sensor. In the case of reflectance at  $180^\circ$  which is the shortest path, the thickness of the sensor is essentially doubled. Any angle of reflectance other than  $180^\circ$  will only increase the apparent thickness further. This is shown in Figure 6-17.

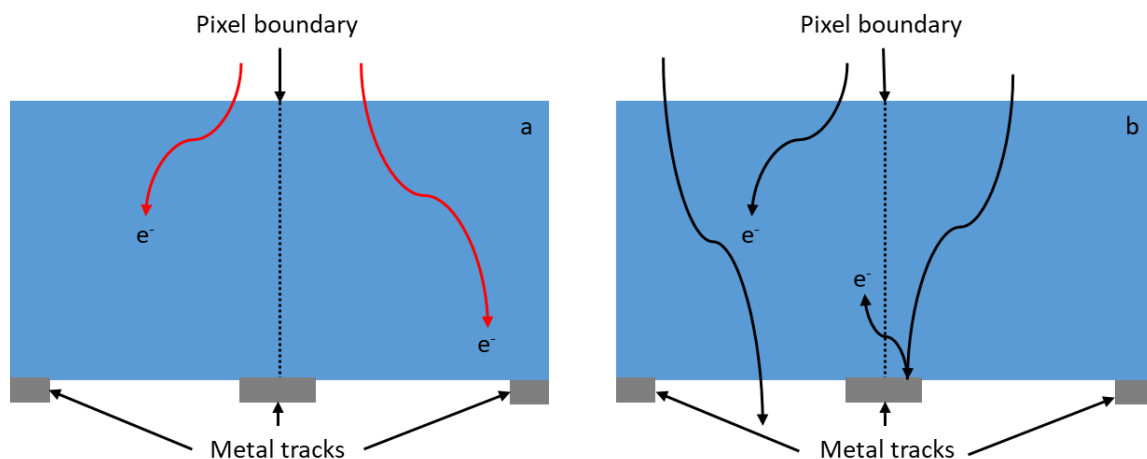


Figure 6-17: Diagram showing different absorption depths of light in the pixel at two wavelengths. In a, the wavelength is relatively short, and the release of an electron occurs at a depth lower than the thickness of the device. In b, the longer wavelength might not interact with the silicon and pass straight through the sensor or reflect off one of the metal tracks and have a second chance of interacting.

Using Equation (6-2), with the value of  $\alpha$  at 940 nm ( $1830 \text{ cm}^{-1}$ ) the absorbance of photons is calculated for light reflected at exactly  $180^\circ$ . As the incoming light passes through the sensor the first time, it interacts with 11  $\mu\text{m}$  of silicon in which generated electrons will contribute to output signal (1  $\mu\text{m}$  of the device thickness is p-wells where any photons generated will not be measured). Statistically, this results in 18.3% of the light generating electrons. This is the total percentage of light which generates electrons which contribute to signal in the case of no reflections. The light

then passes through the p-wells, 1.48% of which generates electrons. When the light is reflected, it interacts with the p-wells again, 1.45% generating electrons. The light then passes through the photo-sensitive area again, a further 14.4% generating electrons. In total, an average of 35.54% of the light will generate electrons throughout the thickness, with 32.7% of this in areas where they will contribute to output signal. In measurements where the light is reflected, 44% of the signal is attributed to the reflected light. The measured 22% variation in signal found between the centres and edges of pixels at 940 nm in Figure 6-16 is smaller than this value, most likely due to light being reflected into other pixels.

Reflected photons were seen to generate signals up to three pixels away from the location of the point source at  $\lambda = 940$  nm, shown in Figure 6-18.

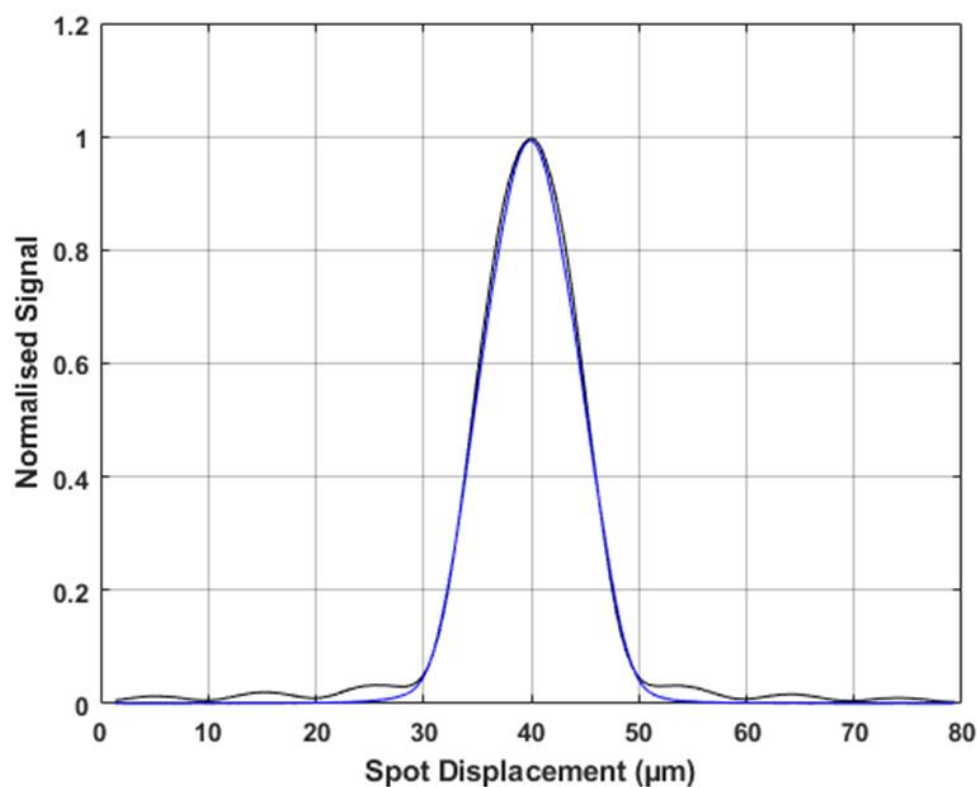


Figure 6-18: Signal recorded in the central pixels of line scans at  $\lambda = 470$  (blue) and  $\lambda = 940$  nm (black). At  $\lambda = 470$  nm, signal is only generated when the point source is adjacent to or within the pixel. At  $\lambda = 940$  nm, signal is measured in this pixel when the point source is on the boundary of two pixels 35  $\mu\text{m}$  away due to reflections.

## 6.6.2 Raster Scanning

To probe the sensitivity of the whole pixel, not just a one-dimensional cross section, the point source was scanned across it in a raster fashion. The point source is centred in the pixel one row above and



one column to the left of the pixel to be scanned. It is then scanned across two pixel widths ( $20\text{ }\mu\text{m}$ ) in steps of  $200\text{ nm}$  in the x-direction, with 100 images captured and the mean image saved. At the end of the  $20\text{ }\mu\text{m}$ , the point source is moved  $200\text{ nm}$  in the y-direction and  $-20\text{ }\mu\text{m}$  in the x-direction, to the starting x co-ordinate. This is repeated until the point source has covered a square region of  $20 \times 20\text{ }\mu\text{m}$ . For each of the mean images, the total signal in the pixel being scanned and the surrounding eight pixels is summed. This is then plotted against the x- and y-coordinate values, and a map of the pixel sensitivity produced.

### 6.6.2.1 Front-Side Illuminated Device

Figure 6-19 shows a raster scan of the front-side illuminated device. The metal tracks which cover the surface can be seen clearly as areas of low signal, as the metal reflects most of the light and cannot enter the sensor. Areas at the corners of the pixels, where the metal is thickest has the lowest values of signal. An estimate for the fill-factor of the sensor can be calculated from the sensitivity map. For this sensor it is around 60%, as the sensitive region is  $\sim 8\text{ }\mu\text{m} \times 7.5\text{ }\mu\text{m}$ .

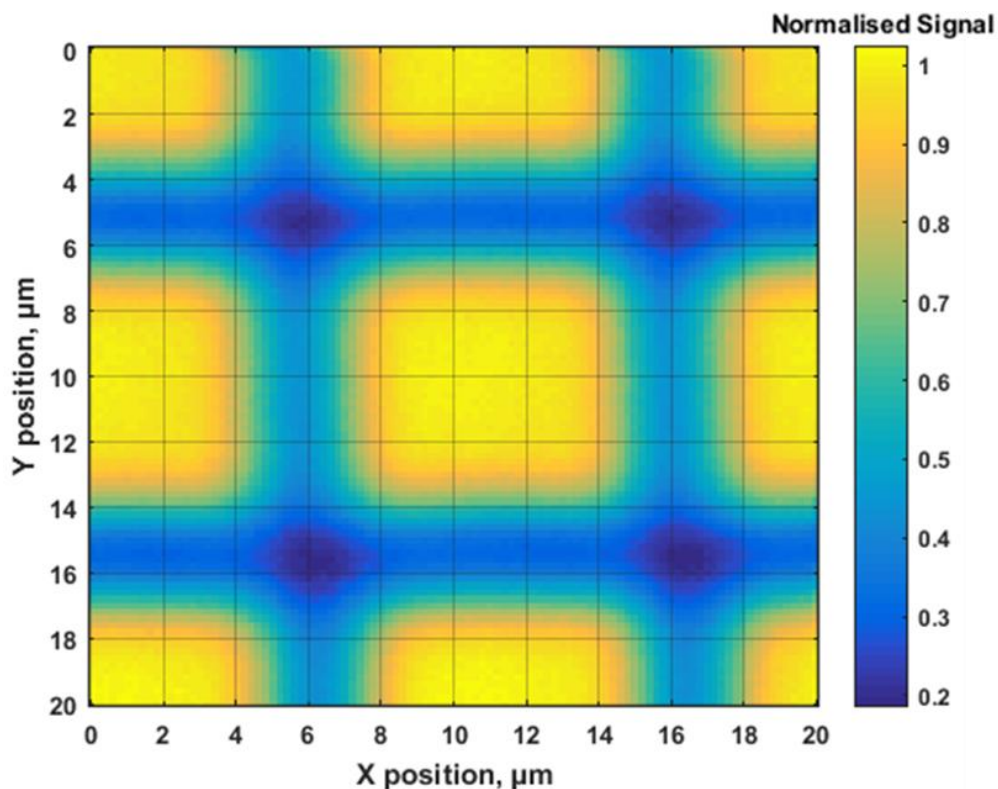


Figure 6-19: Raster scan of a Front Side Illuminated variant of the BSB1 CMOS devices. Pixel boundaries are located at the areas with low signal values.

### 6.6.2.2 Back-Side Illuminated Device

At the shorter wavelengths, the pixel maps are quite uniform and flat. This is to be expected from the data shown in the line scans where the maximum peak to trough value was 1.6%. A raster scan at  $\lambda = 470$  nm is shown in Figure 6-20.

In this figure, the PPD area can be seen as a rectangular shape in the centre of the image. The pixel boundaries where the signal decreases by 1.6% can also be seen. The corners of the pixels show an even larger loss of signal than the boundaries, with the maximum difference at 4.3%. This indicates that at short wavelengths, care should be taken to centre any point sources on the pixel, as the loss of signal at the edges or corners of pixels can be quite pronounced due to unknown reasons still being investigated.

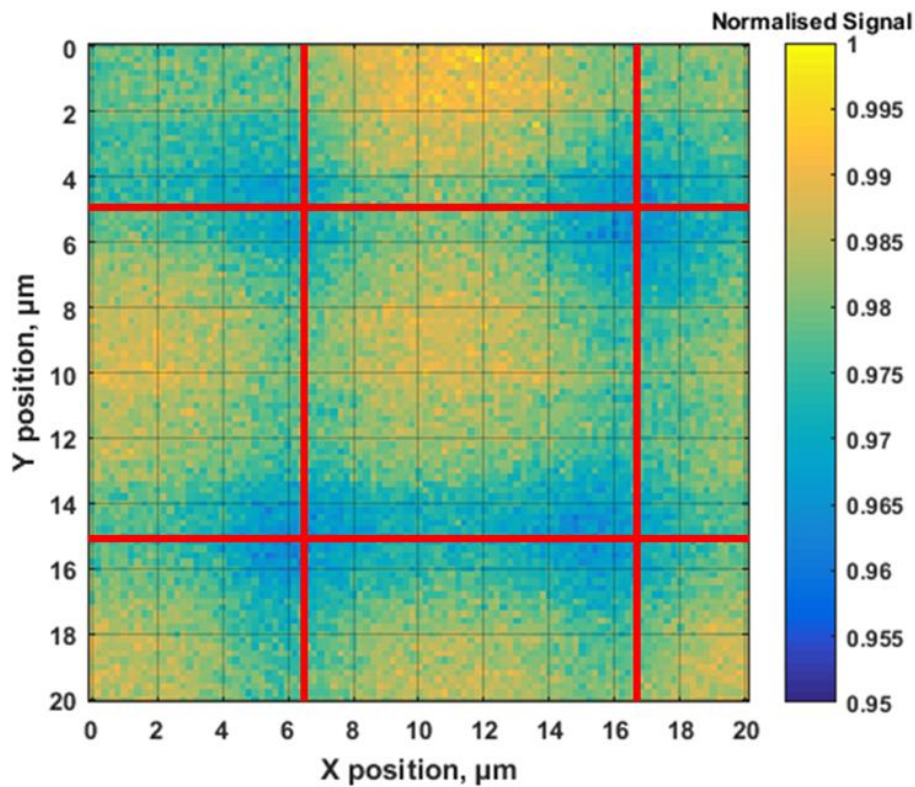


Figure 6-20: Raster scan of a pixel at  $\lambda = 470$  nm. The central pixel's edges are located on the red lines.

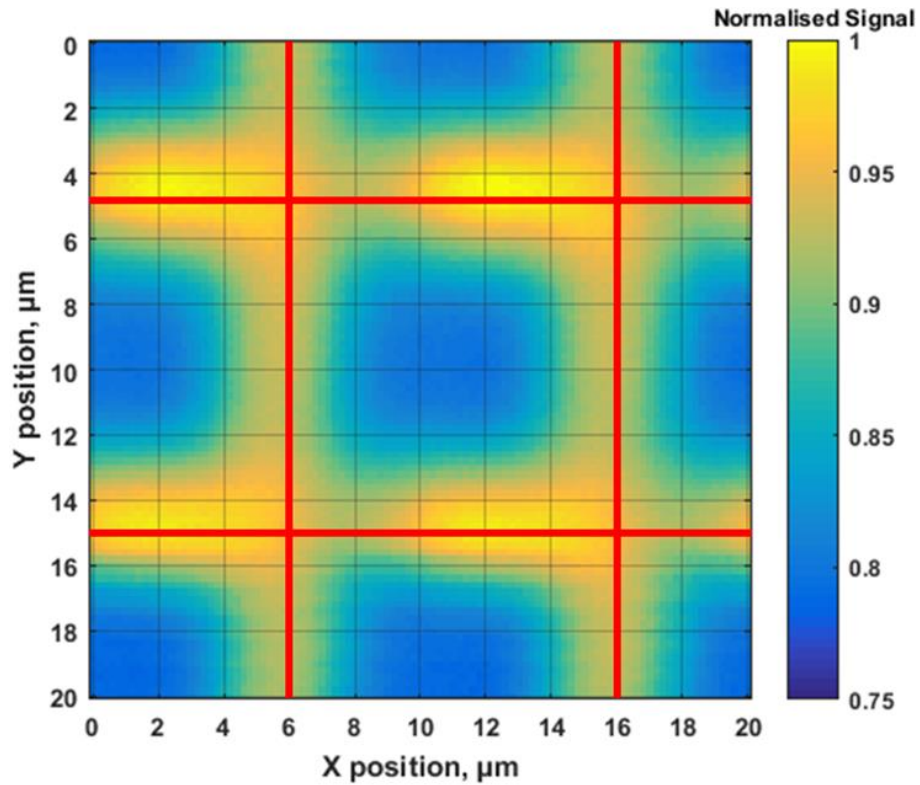


Figure 6-21: Raster scan of a pixel at  $\lambda = 940$  nm. The central pixel's edges are located on the red lines. Pixel boundary lines vary by  $0.4 \mu\text{m}$  from those of Figure 6-20 due to centring misalignments.

Figure 6-21 shows the same scan as Figure 6-20, but at  $\lambda = 940$  nm. As in the line scan of non-uniformity, it shows a difference of 22% in signal from the centre of the pixel to the edges. The metallisation on the front side of the sensor can clearly be seen as areas of increased signal in the image. This is again due to reflections from the metal tracks as the longer wavelengths pass through the sensor without interacting.

When overlaid with the structure of the metal tracks and readout electronics from the design documents, a good agreement is seen between the areas of high signal and the aforementioned structures, shown in Figure 6-22. The location of the highest signals is located under the readout electronics, the transfer gate and transistors, indicating that there may be some interaction there that further increases the signal, such as more reflections due to increased metallisation.

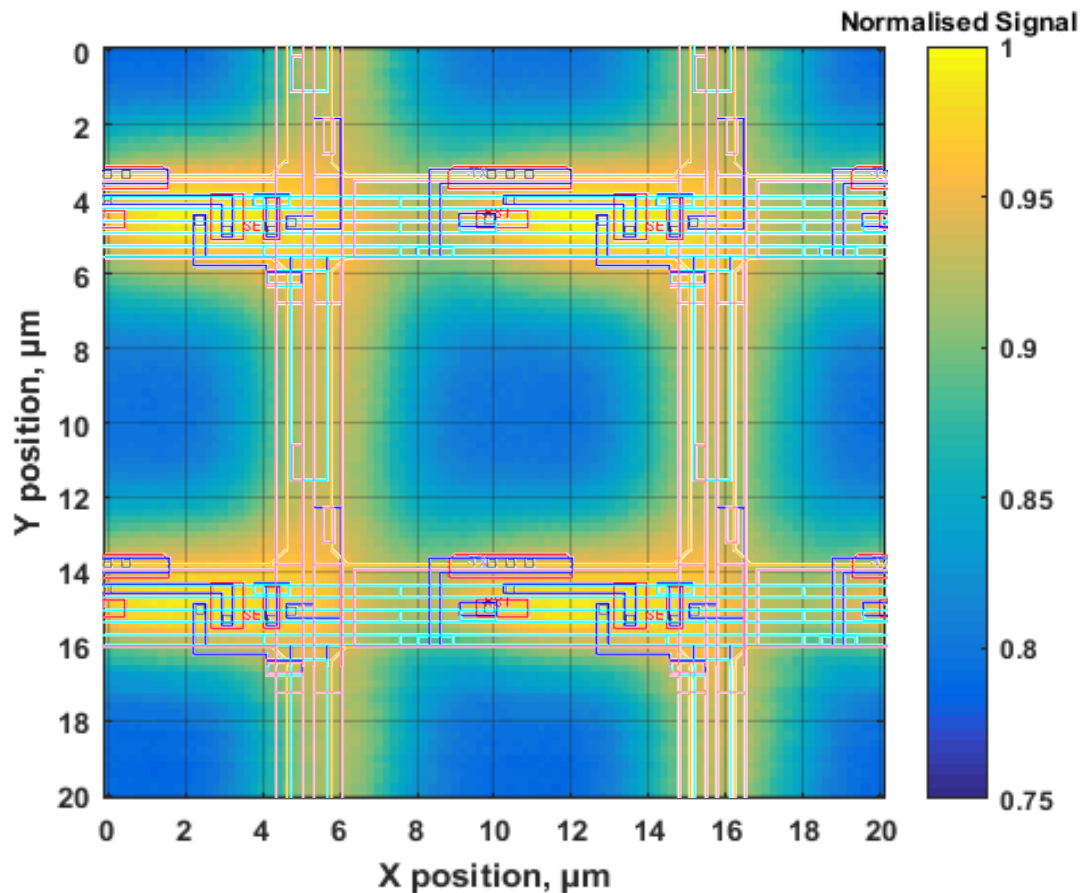


Figure 6-22: Raster scan at  $\lambda = 940$  nm overlaid with the metallisation tracks and readout circuitry of the sensor, showing the alignment with high signal areas.

## 6.7 Point Spread Function

This section describes the measurements of the Point Spread Function of the device, examining the dependence it has on the wavelength of light being measured and the reverse bias applied to the sensor. It details two methods used to determine the PSF as well as a comparison to a Teledyne e2v CCD57.

### 6.7.1 Stationary Point PSF

Initial PSF measurements were made using a stationary point source, of 10  $\mu\text{m}$  diameter, centred over a single pixel. With the point source centred, 1000 images were captured, and the mean of these images calculated. The signal for each of the pixels in the row and column containing the pixel is plotted against the pixel number. The data was then fitted with a Gaussian curve, and the Full Width at Half Maximum used as the metric of the spread of photogenerated charge. These measurements were taken across the full range of wavelengths given in Table 6-1, as well as from 0 V reverse bias to the maximum voltage the device is capable of, -6 V.

### 6.7.1.1 Wavelength Measurements

To test the wavelength dependence, all measurements were run at 0 V reverse bias. Before each measurement, the point source is focussed to account for the change in wavelength.

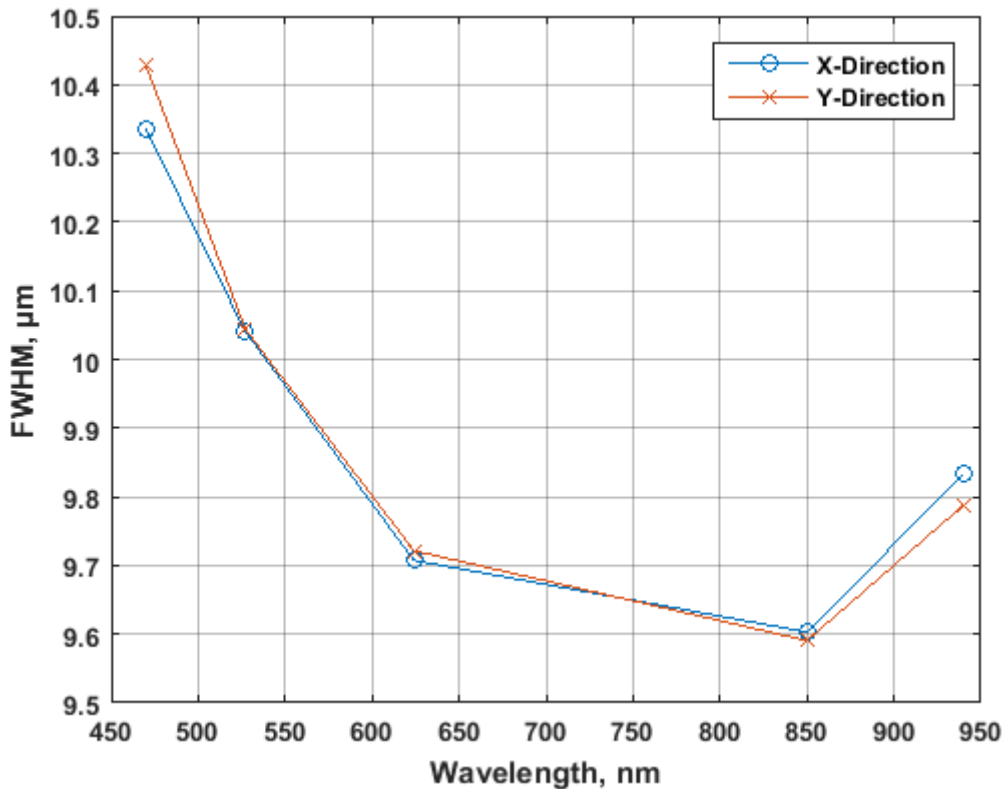


Figure 6-23: Stationary point PSF at 5 wavelengths with 0 V reverse bias in both the x- and y-direction on device W6-2.

With no reverse bias, the depletion region of the sensor does not extend fully to the back side of the device. This means photons of shorter wavelengths will generate electrons in a field free region, allowing them to drift into neighbouring pixels. Longer wavelength photons will be able to penetrate further into the device, increasing the chance that they generate electrons inside the depletion region. This leads to the trend seen in Figure 6-23 where the FWHM decreases as wavelength increases. The increase in FWHM at  $\lambda = 940$  nm is due to reflections from the metal tracks which was discussed in the previous section.

The difference in the FWHM in the x- and y-directions is likely due to the readout circuitry being scanned over when the point source is moved in the y-direction.

### 6.7.1.2 Reverse Bias Measurements

Figure 6-24 shows the results for stationary spot PSF measurements taken at  $\lambda = 470$  nm. When there is no reverse bias, the depletion region is shallower. Since photons at this wavelength are absorbed in a very small distance, most of the photogenerated electrons will be created outside of this depletion region and can drift to neighbouring pixels.

As the reverse bias is increased, the depletion region extends towards the back of the device. This shortens the distance that the electrons must travel through non-depleted silicon in order to reach an area of depletion. Since electron drift is a random process, this smaller distance increases the likelihood that an electron will enter the depletion region of the same pixel that it was generated in. As the depletion depth is increased, the probability of this occurring is increased, thus lowering the PSF of the sensor.

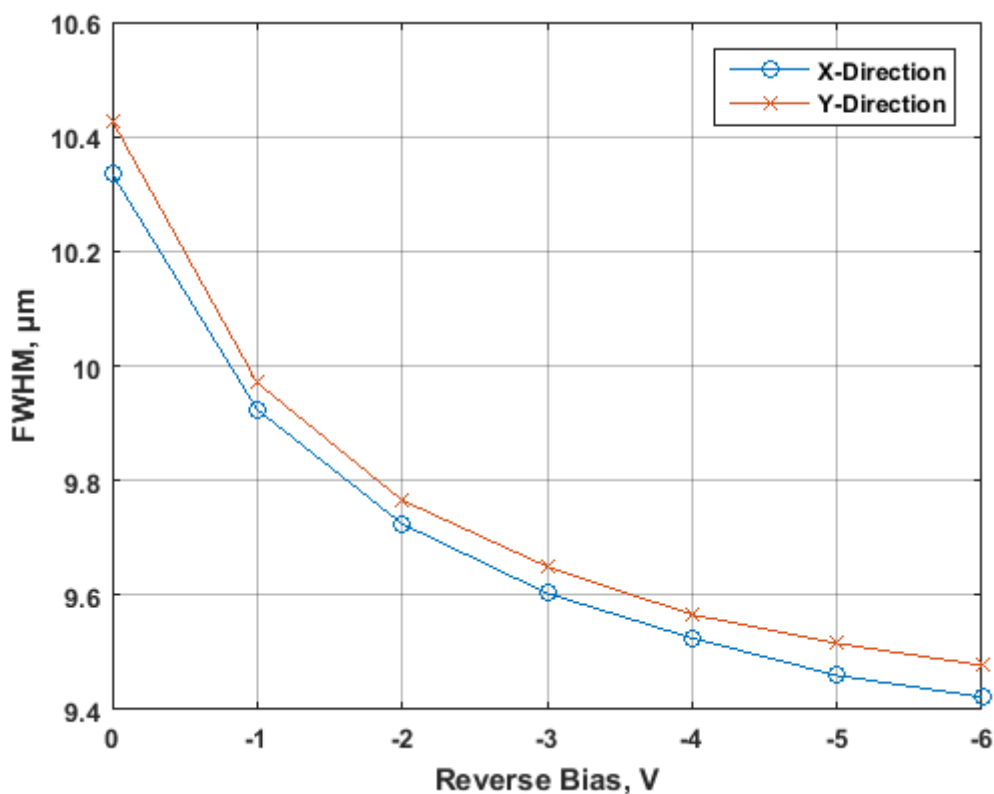


Figure 6-24: Stationary point PSF at  $\lambda = 470$  nm in both the x- and y-direction with increasing reverse bias.

The data follows the expected trend of decreasing PSF with increasing reverse bias. An improvement of 9% in the measured PSF is achieved from 0 V reverse bias to the maximum of -6 V. Using Equation (6-1), the depletion depth can be calculated. The specifications of the sensor are  $N_A = 1.3 \times 10^{13}$ ,

$V_{pin} = 1.5$  V, fully depleting 12  $\mu\text{m}$  at a reverse bias of about -2 volts. Above this value the graph begins to level off, and the reduction in the FWHM is due to over-depletion.

Figure 6-25 shows the results for reverse bias tests at all 5 wavelengths used. All of the wavelengths tested show a decrease in the FWHM as reverse bias is increased. As the wavelength increases, the difference between the FWHM at 0 V reverse bias and -6 V decreases as the longer wavelengths have a higher probability of generating electrons in the shallower depletion region. The differences are shown in Table 6-2.

Wavelength, nm	Change in FWHM, $\mu\text{m}$
470	0.95
527	0.87
624	0.69
850	0.34
940	0.27

*Table 6-2: Difference between the FWHM measured at 0 V and -6 V reverse bias for each wavelength.*



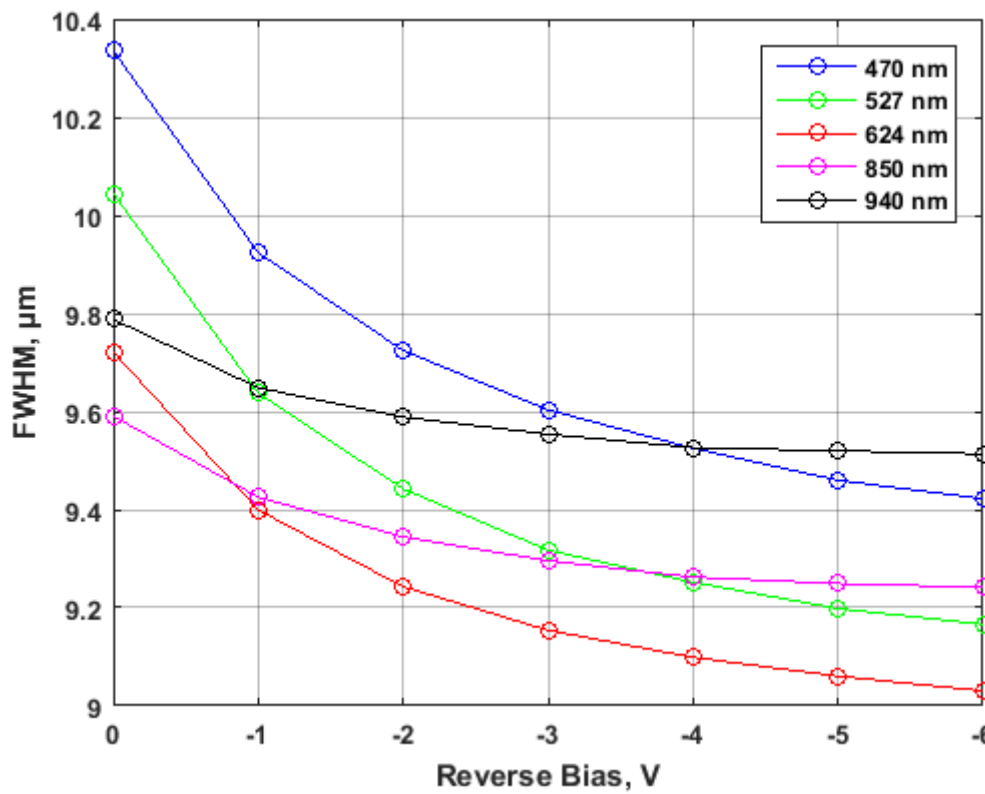


Figure 6-25: Measured FWHM across all wavelengths at a range of reverse bias voltages with a 10 $\mu$ m point source. All measurements taken in the x-direction.

### 6.7.2 Virtual Knife Edge PSF

The virtual knife edge technique is a way of measuring the PSF of a sensor with a moving point source [8]. It is based loosely on the Foucault knife-edge technique used for measuring mirror aberration.

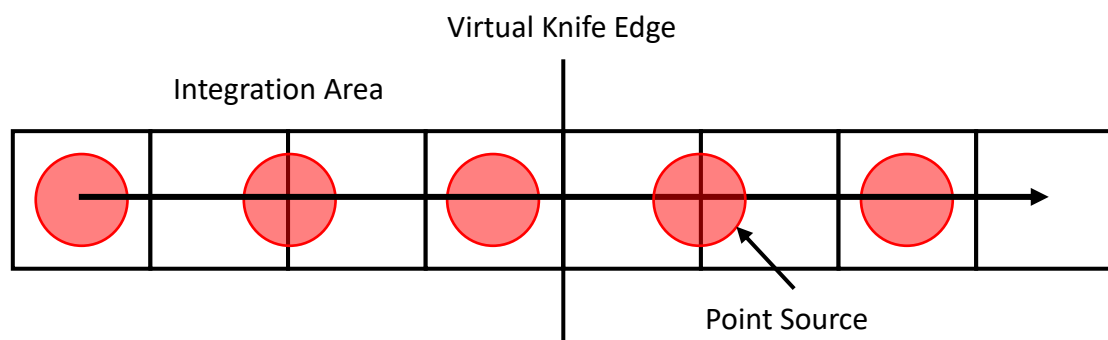


Figure 6-26: A representation of the Virtual Knife Edge technique. The point source begins in the leftmost pixel of the diagram and is scanned across all 8 pixels in small steps, with only the signal in the integration area being measured.

Instead of using a physical object to obstruct the beam of light, the image area is instead divided into two sections – one in which the signal generated is measured, known as the integration area, and one in which it is not. The boundary between these two areas is known as the Virtual Knife Edge because it acts as though there is a perfectly sharp edge at this point, blocking all light to the sensor. At the start of the test, the beam is located in the integration area and moved in steps of 500 nm across the 4 measured pixels and the 4 which are not measured. At each point, 100 images are taken, and the mean image calculated. This is shown in Figure 6-26.

From the mean images, the total signal in the integration area is calculated and plotted against the translation stage displacement. The differential of the signal-displacement graph is then calculated and plotted. As with the stationary point PSF, the resulting graph is fitted with a Gaussian curve and the FWHM taken as the PSF value.

A 1  $\mu\text{m}$  point source was used for all VKE tests as this gives the most repeatable results and smoothest Gaussian curves.

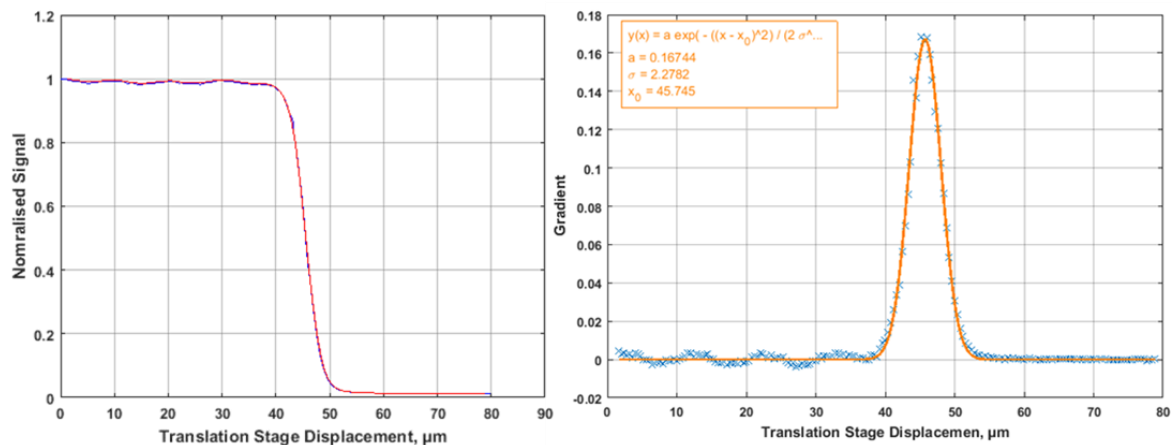


Figure 6-27: Data used to calculate PSF from VKE measurements. The left figure shows the total signal measured in the integration area, and the right shows the differential of the signal graph.

### 6.7.2.1 Reverse Bias Measurements

As with the measurements taken using the stationary point technique, PSF was measured using the VKE technique whilst changing the reverse bias applied to the sensor. Results are shown in Figure 6-28.

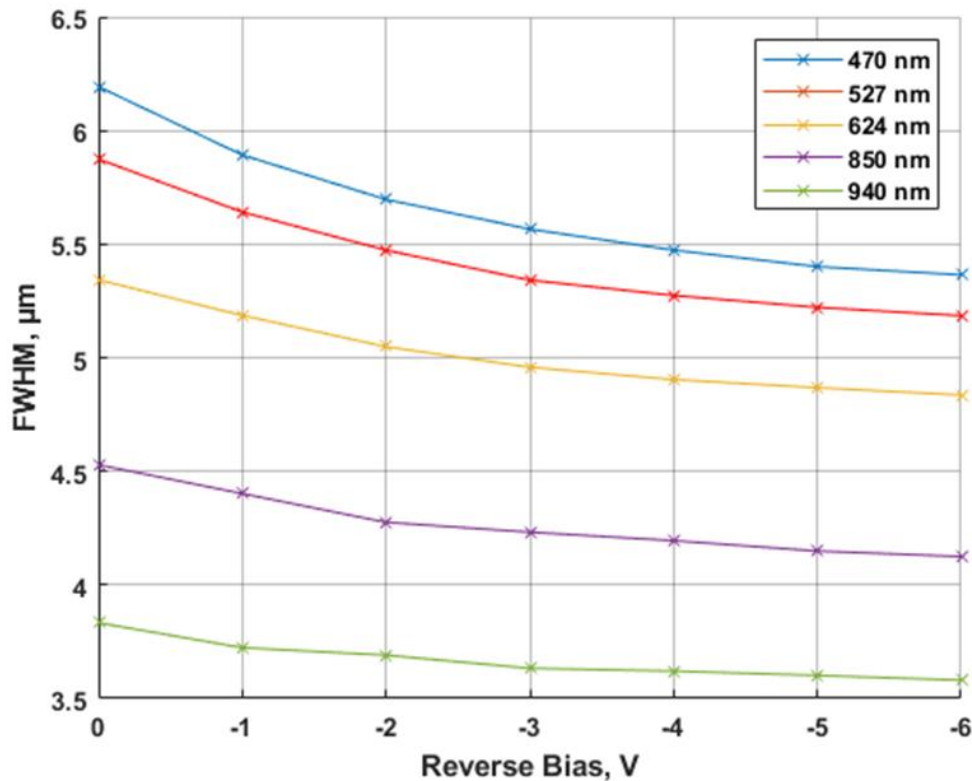


Figure 6-28: Comparison of PSF values for different wavelengths with varying reverse bias voltages. Results are shown for x-direction only, measured with a  $1\mu\text{m}$  wide point source.

The results for the VKE tests of the PSF show the expected trend of decreasing the value of the PSF as both wavelength and reverse bias increase. As with the stationary point technique, the reverse bias has the greatest effect on the shortest wavelength (470 nm) and the smallest effect on the longest wavelength (940 nm).

An advantage of the VKE technique that can be seen in the results is that it is less affected by reflections in the way that the stationary point technique is. It also provides far more datapoints on which to fit a Gaussian curve, increasing the R number and giving a truer fit.

### 6.7.2.2 Wavelength Measurements

Comparisons of the measured PSF in the x- and y-directions were made at multiple wavelengths to investigate the wavelength dependence of PSF using the VKE technique.

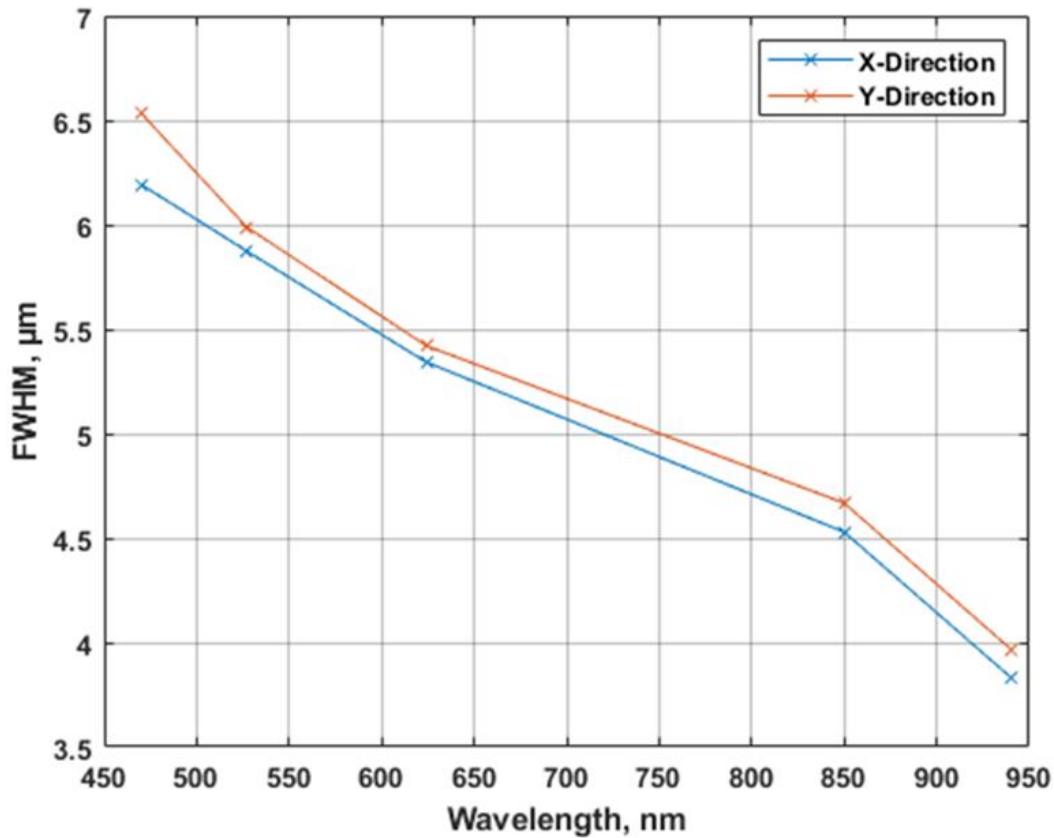


Figure 6-29: Wavelength dependence of PSF in both x and y directions. All tests run at 0V reverse bias.

Using the VKE technique to test the wavelength dependence of the PSF shows the expected trend with no reverse bias of decreasing PSF with increasing wavelength, as in Figure 6-29. Again, the PSF is slightly greater in the y-direction than the x-direction, as the readout transistors are scanned over by the point source when movement is in the y-direction.

## 6.8 Comparison with CCD57

To be able to claim the new technology as successful, it must be compared to the established existing technology. Since there are no other CMOS sensors capable of reverse bias being produced, the Te2v CCD57 [9] was chosen, shown in .

The CCD57 is a back-side illuminated, frame transfer sensor comprised of  $512 \times 512$ ,  $13 \mu\text{m}$  square pixels. It is fully depleted and is  $13 \mu\text{m}$  thick, very close to the thickness of the BSB1 CMOS devices.

For all tests run on the device it was windowed down to a  $50 \times 50$  region of interest to allow for a larger frame rate. This greatly reduced any dark signal effects and increased data capture rate.



Figure 6-30: Photograph of the CCD57 mounted on the PCB with connectors to external power sources and data transmission lines.

The supplied voltages were optimised before any PSF measurements were done via PTC measurements and CTI measurements.

Although the pixels are slightly larger than those of the BSB CMOS device, no extra data manipulation is needed. This is because the VKE technique is only measuring the interface between two pixels which is the same size no matter how large the pixel area.

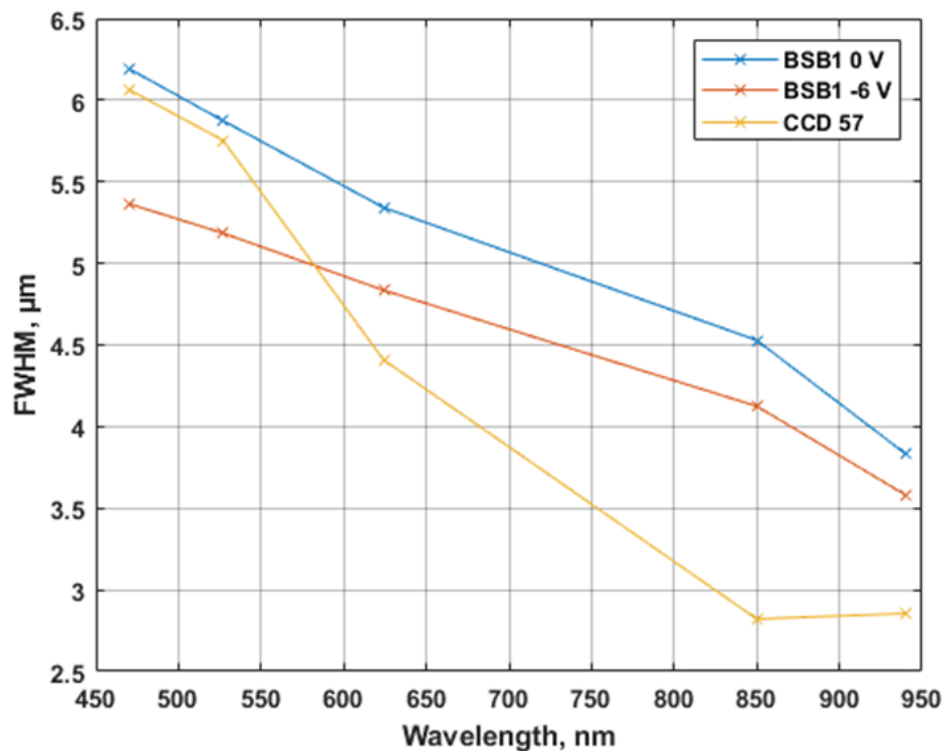


Figure 6-31: Comparison of measured PSF in the BSB CMOS device, with and without reverse bias, and CCD 57 with full depletion. The CMOS data is for movement in the x-direction, whilst the CCD data is in the serial direction.

Figure 6-31 shows the measured PSF in the BSB CMOS sensor, with no reverse bias and with maximum bias, and the CCD 57. With no reverse bias (0 V) on the CMOS sensor, the CCD achieves a lower PSF value across all wavelengths measured. When reverse bias is applied to the CMOS sensor, it has a lower PSF than the CCD at shorter wavelengths, but at 624 nm and above, the CCD has a lower measured PSF. This is likely due to the reflection of light at longer wavelengths in the CMOS sensor. Although the two devices are of a similar thickness, the CCD exhibits a lower effect from reflected light off its polysilicon gates. This may be due to the more homogeneous layout of the gates on the CCD when compared to metal tracks of the CMOS sensor, as almost all the front side of the CCD has gates running across it, whereas the CMOS sensor only has tracks around the edges of the pixels.

## 6.9 Conclusions

The characterisation done in this chapter indicate that the concepts used in the BSB CMOS devices are correct and are working as intended, and that full depletion in an almost standard CMOS device has been achieved.

Inter-pixel non-uniformity is low, with less than 1 % discrepancy between peak pixel values when measured with a point source. This shows that the extra processing step of adding the DDE to a pixel has very little effect on the performance of individual pixels. It was also shown that there is no wavelength dependence on inter-pixel non-uniformity at similar signal levels.

Intra-pixel non-uniformity was found to be minimal at shorter wavelengths with a maximum of 1.6 % found at 470 nm from the maxima in the centre of the pixels to the minima at the boundaries between two. At longer wavelengths, when the absorption depth is greater than the thickness of the sensor, the intra-pixel non-uniformity becomes more pronounced. At 940 nm, the difference between the maxima and minima was found to be  $\approx 22$  %. The maxima at longer wavelengths are found at the edges of the pixels, and the minima at the centre of the photodiodes. This is due to reflections from the metallisation on the front side of the sensor, increasing the chance of the light

being measured. The secondary measuring of the light does not always take place in the pixel the light was first incident upon, causing a spread of signal over many pixels. This must be considered when performing any measurements on long wavelength light sources with a CMOS device. For instance, in the case of precision astronomy, it is important to know where in the pixel the point source is located, as the signal may be measured higher than it is if it is on the boundary between two pixels – up to 44% if all of the photons are reflected directly back into a sensor of this thickness and design. It can also lead to shape deformation as the charge is spread among several pixels. The thickness of the device must be chosen for specific wavelengths to mitigate this where possible.

In PSF measurements, the application of reverse bias was found to reduce the spreading of charge considerably, with an improvement of almost 10% from 0 V to -6 V at 470 nm in stationary point measurements. The improvements diminish as wavelength increases as would be expected as the absorption depth increases, down to about 3% at a wavelength of 940 nm. Virtual Knife Edge measurements showed similar reductions in the measured PSF as the stationary point method but was not affected by reflections to the same degree. An improvement of 13% was found at 470 nm between 0 V and -6 V reverse bias using this method, and 7% at 940nm.

In comparison with CCD 57, the BSB CMOS sensor exhibits similar PSF results when reverse biased. At the two shortest wavelengths, the CCD was found to have a slightly higher PSF than the CMOS, but the trend is reversed at wavelengths greater than 624 nm. This is thought to be due to the reflections from the metal tracks in the CMOS sensor.

## 6.10 References

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## 7 Conclusions and Further Work

The work presented in this thesis focussed on characterising the BSB1 CMOS sensors and ensuring that the modifications made to differentiate it from a standard pixel layout did not inhibit the device performance. Alongside this, image lag was measured and a novel method for its reduction was investigated. Non-uniformities, both between pixels and within a pixel itself, were examined as well as the point spread function of the device to verify that full depletion was achieved.

### 7.1 Sensor Characterisation

Chapter 4 describes the baseline characterisation of a number of metrics of the sensors. These include the leakage current, gain, full well capacity, linearity and image lag.

The leakage current of the devices was measured to obtain the maximum values for the reverse bias voltage that each device variant could operate. It was found that the higher the DDE implant dose, the higher the reverse bias which could be applied. It was also found that a higher pinning voltage allowed a higher reverse bias.

The gain and full well capacities were obtained via the photon transfer curve. The results indicate that the gain is almost unchanged by the addition of the DDE and application of reverse bias. Whilst the full well capacities of the variants with smaller DDEs were unchanged with reverse bias, the variants with larger DDEs suffered from charge sharing effects between pixels in the absence of reverse bias. The full well capacities of these devices fully recovered with the application of reverse bias, due to the lowering of the potential in the DDE area, removing the conducting path between pixels.

Both linearity and image lag were found to be unaffected by the application of reverse bias. For all devices, the linearity stayed constant throughout the range of voltages tested. Image lag was found to improve quite considerably with the addition of the DDE, although the reasons for this are unknown.

## 7.2 Image Lag

Chapter 5 was dedicated to the measurement of image lag in device W6-2. Tests on multiple parameters including transfer gate high voltage, transfer gate 'on' time and floating diffusion reset voltage were conducted. The location of charge at the end of the transfer period was simulated in order to confirm the theory of charge spill-back. The second half of the chapter focusses on a novel lag reduction technique by applying a multi-level transfer gate voltage.

### 7.2.1 Single Level Transfer Gate Voltage

Electrons are transferred from the photodiode to the floating diffusion by applying a voltage to the transfer gate. The magnitude of this voltage has a profound effect on the proportion of the charges transferred. A high value for this voltage results in low levels of measured image lag at low signal levels due to the higher potential drawing electrons across. Low voltages result in higher measured image lag at low signals, but lower measured image lag at higher signal values. This is due to the onset of charge spill-back occurring at lower signal levels for high voltages. The transfer gate voltage must therefore be optimised for the signal levels expected whilst imaging.

As the transfer gate 'on' time is increased, the measured image lag decreases. Increased time allows electrons further from the transfer gate more time to drift across, reducing image lag. The reduction in image lag gained from having a longer transfer time suffers from diminishing returns, so a balance must be found between reducing image lag and the framerate of the device.

The floating diffusion reset level was altered to test the theory of charge spill-back. Reducing the reset level did indeed reduce the signal size needed before the image lag became spill-back dominated. The charge-to-voltage factor was used to confirm the difference between the reset voltages corresponded to the number of electrons stored on the floating diffusion.

TCAD simulations showed that the charge at the end of the transfer period was spread under the entire length of the transfer gate when a high voltage was applied to it, and that the charge was entirely contained in the floating diffusion when the transfer gate voltage was low.

### 7.2.2 Multi-Level Transfer Gate Voltage

With minor modifications to the external circuitry, it was possible to apply more than one transfer gate high voltage in a single readout phase. With more than one level, it is possible to combine the advantages of both high and low transfer gate voltages in a single transfer with none of the drawbacks.

For the two-level transfer gate voltage tests, it was found that a short application of a high voltage followed by a long lower voltage level resulted in the lowest measured image lag. Charge transfer was found to be exponential, so a high voltage of a short duration draws the majority of electrons into the floating diffusion, whilst the long duration medium voltage allows electrons to drift from the far side of the floating diffusion. A longer middle voltage also gives the charges time to move from under the transfer gate. The initial high voltage should be kept high, whilst the middle voltage is just above the threshold voltage of the transfer gate.

Using a ramped down voltage on the transfer gate gives similar results to the two-level transfer gate, with advantages of both high and low transfer gate voltages. The measured image lag is slightly lower than that of the two-level regime, but is slightly harder to implement, requiring more modifications and characterisation.

The multi-level transfer gate method proved to achieve lower lag levels than the standard single-level used in all current CMOS sensors. This method is an easy and cheap way to decrease image lag in off the shelf sensors, with no need to design new ones.

## 7.3 Non-Uniformity and PSF

Chapter 6 described the measurement of the non-uniformity of W6-2, as well as tests to ensure that full depletion was achieved by the device.

### 7.3.1 Inter-Pixel Non-Uniformity

The peak signal value for each pixel in a number of rows was measured and compared to the rest of the row to determine the variation. This method differs from the normal method of flat field illumination as it avoids any charge sharing from neighbouring pixels and gives a more representative value. The largest variation was found to be around 1% pixel to pixel, indicating a very high uniformity between pixels. The results showed there was no dependence on wavelength for the uniformity, and that the DDE has no effect on it.

### 7.3.2 Intra-Pixel Non-Uniformity

Intra-pixel non-uniformity was found to be low at short wavelengths as the majority of photons could not penetrate the silicon far enough to reach the features on the front side. The areas of maximum non-uniformity in signal found within pixel had a difference of about 1.6%.

At longer wavelengths, the photons were not absorbed in the 12  $\mu\text{m}$  thickness of the device and so could reflect off the metal tracks which run across the front side of the device. This resulted in a difference in signal measured in the middle of the pixel and the boundary of the pixel of 22%. This was confirmed theoretically using the absorption depth of the photons and the thickness seen by a photon passing through 11  $\mu\text{m}$  and 22  $\mu\text{m}$  of silicon. The wavelength of the light must therefore be taken into consideration when measuring with thin CMOS devices as the signal can be artificially inflated depending on where the point source is located within the pixel.

### 7.3.3 Point Spread Function

The point spread function was measured through two methods at varying reverse biases and wavelengths to verify full depletion had been achieved by the device. Results showed that the PSF of the sensor decreased as the reverse bias was increased, confirming full depletion had been reached. Results also showed the PSF decreases as the wavelength increases, which is expected when absorption depth is taken into consideration. When compared with a CCD of similar physical

attributes, the results were largely similar, showing that the device is capable of full depletion like a CCD.

## 7.4 Future Work

The work in this thesis has demonstrated that the BSB1 devices function as well as a standard CMOS sensor in all of the basic metrics used to test a device. It however has the advantage that it can be fully depleted, allowing thicker devices with no increase to charge diffusion. A thicker device can improve the quantum efficiency, closing the gap on one of the main advantages of a CCD. The applications for this new technology are far-reaching. Virtually any camera which currently uses CMOS technology can incorporate it. Many areas which currently use CCDs can substitute them for CMOS sensors of this type and gain the benefits which are inherent to CMOS. Since the alterations to the pixel structure are minimal and fabrication only involves a few extra steps, it can be implemented very easily with little extra development to current pixel designs.

Future work to build on the foundations laid by this thesis should focus mainly on the design, fabrication and characterisation of a large format CMOS sensor with the DDE implant, with a thickness of up to 100  $\mu\text{m}$ . The wavelength corresponding to 100  $\mu\text{m}$  absorption depth is around 1000 nm, in the near infrared band. This is an important band for astronomy as it is used for measuring redshift and the temperature of objects. A proof of concept at this thickness would lead the way to applying the technology to other CMOS sensors and would push CMOS closer to replacing the CCD as the de facto standard of solid-state image sensors in precision astronomy.